SPECTRUM DIGITAL INCORPORATED

TMS320DM357 Evaluation Module

Technical Reference

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TMS320DM357 Evaluation Module Technical Reference

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About This Manual

This document describes the board level operations of the DM357 Evaluation Module (EVM). The EVM is based on the Texas Instruments DM357 Processor.

The DM357 Evaluation Module is a table top card that allows engineers and software developers to evaluate certain characteristics of the DM357 processor to determine if the processor meets the designers application requirements. Evaluators can create software to execute on board or expand the system in a variety of ways.

Notational Conventions

This document uses the following conventions.

The DM357 Evaluation Module will sometimes be referred to as the DM357 EVM or EVM.

Program listings, program examples, and interactive displays are shown in a special italic typeface. Here is a sample program listing.

equations
!rd = !strobe&rw;

Information About Cautions

This book may contain cautions.
This is an example of a caution statement.
A caution statement describes a situation that could potentially damage your software, or hardware, or other equipment. The information in a caution is provided for your protection. Please read each caution carefully.

Related Documents, Application Notes and User Guides

Information regarding TMS320DM357 technology can be found at the following Texas Instruments website:

http://www.ti.com

Table 1: Manual History

Revision	History
A	Alpha Release

Table 2: Board History

PWB Revision	History
A	Alpha Release

Chapter 1

Introduction to the DM357 EVM

Chapter One provides a description of the DM357 EVM along with the key features and a block diagram of the circuit board.

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1.1 Key Features

The DM357 EVM is a standalone development platform that enables users to evaluate and develop applications for the TI DM357 processor. Schematics, logic equations and application notes are available to ease hardware development and reduce time to market.

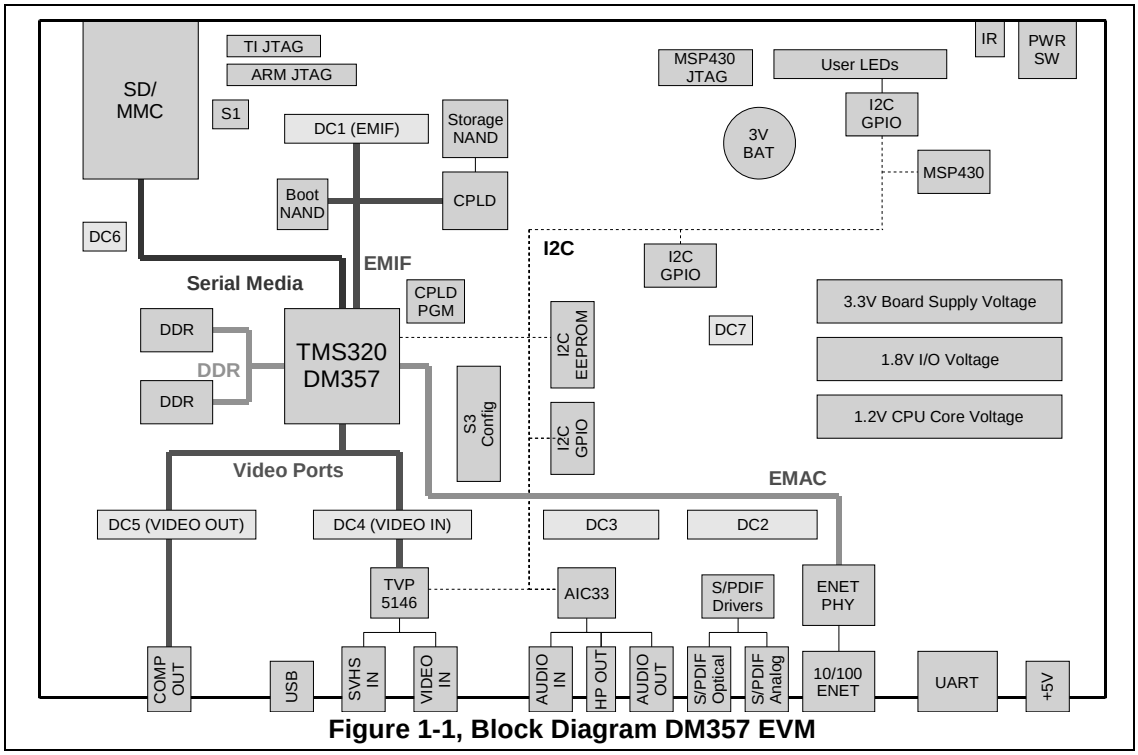

Figure 1-1, Block Diagram DM357 EVM

The EVM comes with a full complement of on board devices that suit a wide variety of application environments. Key features include:

- A Texas Instruments DM357 processor with an ARM processor operating up to 270 Mhz. and H.264/MPEG4/JPEG coprocessor
- 1 video input port, supports composite or S video
- 1 video DAC outputs - composite
- 256 Mbytes of DDR2 DRAM
- UART, Media interface (SD card, MMC)
- 64 Mbytes NAND Flash for BOOT, 2 gigabyte NAND storage NAND
- AIC33 stereo codec
- USB2 Interface

- 10/100 MBS Ethernet Interface
- IR Remote Interface, real time clock, via MSP430
- Configurable boot load options
- JTAG emulation interface with 1.8 volt to 3.3 volt translators
- 8 user LEDs
- Single voltage power supply (+5V)
- Expansion connectors for daughter card use

1.2 Functional Overview of the DM357 EVM

The DM357 on the EVM interfaces to on-board peripherals through the 16-bit wide EMIF peripheral interface pins. The DDR2 memory is connected to its own dedicated 32 bit wide bus. The EMIF bus is also connected to the boot NAND, storage NAND, and daughter card expansion connectors which are used for add-in boards.

On board video decoder for composite or s-video and on chip encoders interface video streams to the DM357 processor. One decoder and 1 on chip DAC channel for composite out are standard on the EVM. On screen display functions are implemented in software on the DM357 processor.

An on-board AIC33 codec allows the CPU to transmit and receive analog audio signals. The I^2C bus is used for the codec control interface, while the McBSP controls the audio stream. Signal interfacing is done through 3.5mm audio jacks that correspond to microphone input, line input, and line output. The codec can select the line input as the active input.

The EVM includes 8 LEDs, IR interface, and Real time clock which can be used to provide the user with interactive feedback. These interfaces are implemented via software on a MSP430 and are accessed by reading and writing to the I^2C registers.

SD/MMC Media card and ethernet MAC interfaces are integrated peripheral on the DM357 processor exploiting its system on a chip architecture.

An included 5V external power supply is used to power the board. On-board switching voltage regulators provide the +1.2V CPU core voltage and +3.3V for peripherals and +1.8V memory and DM357 I/O. The board is held in reset until these supplies are within operating specifications.

Code Composer Studio communicates with the EVM through an external emulator via the 14 TI or 20 pin ARM external JTAG connector.

1.3 Basic Operation

The EVM is designed to work with TI's Code Composer Studio IDE™, or standard GDB tool environments. Code Composer communicates with the board through an external JTAG emulator.

Detailed information about the EVM including examples and reference material is available on the EVM's CD-ROM.

1.4 Memory Map

The DM357 processor has a large byte addressable address space. However, some limitations to byte addressing may be present depending on the board to device peripheral interconnection. Program code and data can be placed anywhere in the unified address space. Addresses are multiple sizes depending on hardware implementation. Refer to the appropriate device data sheets for more details.

The memory map shows the address space of a DM357 processor on the left with specific details of how each region is used on the right.

The part incorporates a dual EMIF interface. One dedicated EMIF directly interfaces to the DDR2 memory. The other EMIF has 4 separate addressable regions called chip enable spaces (CE2-CE5). The boot NAND Flash, or daughter card are mapped into CE2 space and selectable via J4. Daughter cards use CE2 and CE3. When CE2 is used for daughter card interfacing J4 must be set appropriately. CE4 is used to interface to storage NAND.

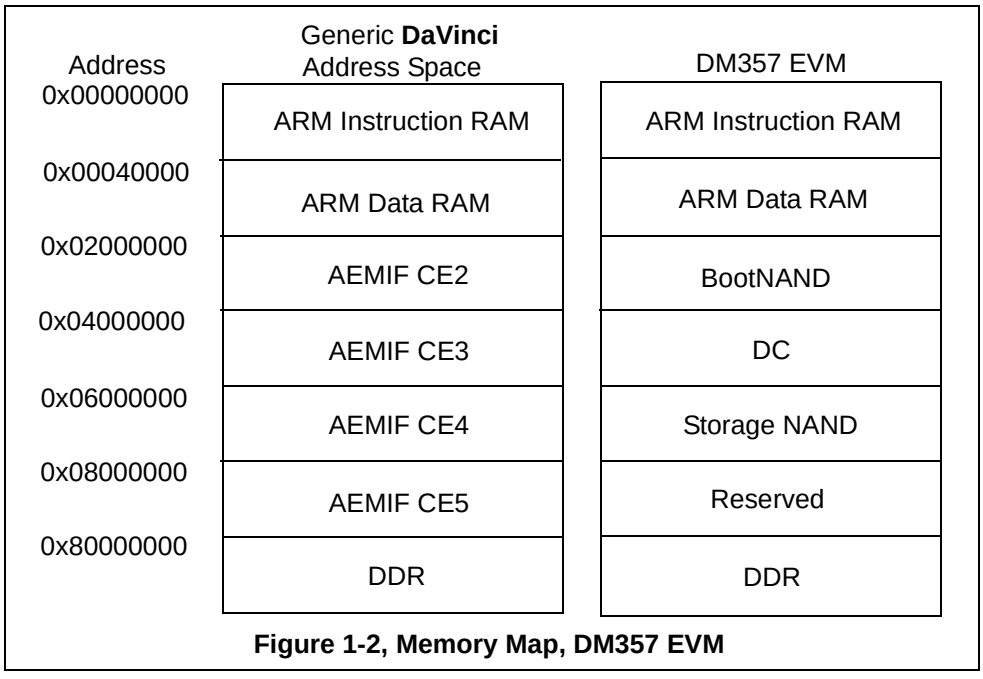

Figure 1-2, Memory Map, DM357 EVM

1.5 Configuration Switch Settings

The EVM has a single 10 position configuration switch that allow users to control the operational state of the processor when it is released from reset. The configuration switch is labeled S3 on the EVM board.

Switch S3 configures the boot mode that will be used when the processor starts executing. By default the switches are configured to EMIF boot (out of 8-bit NAND Flash) in little endian mode. The settings for switch S3 in chapter 3.

1.6 Power Supply

The EVM operates from a single +5V external power supply connected to the main power input (J14), a 2.5 MM. barrel-type plug. Internally, the +5V input is converted into +1.2V, +1.8V and +3.3V using Texas Instruments swift voltage regulators. The +1.2V supply is used for the CPU core while the +3.3V supply is used for the CPU's I/O buffers and other chips on the board. The +1.8 volt supply is used for DM357 I/O, low voltage memory, and peripherals, and DDR2 memory.

There are four power test points on the EVM; TP14, TP25, TP26, and TP43. These test points provide a convenient mechanism to check the EVM's multiple power supplies. The table below shows the voltages for each test point and what the supply is used for.

Table 1: Power Test Points

Test Point	Voltage	Voltage Use
TP43	+1.2 V	DM357 Core
TP25	+1.2 V	DM357 Core/Power Down
TP26	+1.8 V	DDR2 Memory, CPU I/O, and logic
TP14	+3.3V	CPU I/O and logic

Chapter 2

Board Components

This chapter describes the operation of the major board components on the DM357 EVM.

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2.1 EMIF Interfaces

A separate 16 bit EMIF with four chip enables divide up the address space and allow for asynchronous accesses on the EVM. The EVM has a dedicates chip enables. CE2 is used for the boot NAND Flash. Both CE2 and/or CE3 can be routed to the daughter card interface connectors. CE4 is used for storage NAND flash.

Table 1: EMIF Interfaces

Chip Select	Function
CE2	Boot NAND Flash (see JP4 definition)
CE2	Daughter Card Interface (see JP4 definition)
CE3	Daughter Card Interface
CE4	Storage NAND Flash
CE5	Reserved

2.1.1 DDR2 Memory Interface

The DM357 device incorporates a dedicated 32 bit wide DDR2 memory bus. The EVM uses two gigabit 16 bit wide memories on this bus, for a total of 256 megabytes of memory for program, data, and video storage. The internal DDR controller uses a PLL to control the DDR memory timing. The interface supports rates up to 166 Mhz., and is clocked on differential edges for optimal performance. Memory refresh for DDR2 is handled automatically by the DM357 internal DDR controller.

2.1.2 Boot NAND Flash Interface

The DM357 has 64 megabytes of Boot NAND Flash mapped into the CE2 space. This NAND Flash memory is used for boot loading. The CE2 space is configured as 8 bit wide for NAND flash usage.

2.1.3 Storage NAND Interface

The EVM interfaces to 2 gigabytes of storage NAND flash mapped to CE4 space. CE4 is configured to 8 bit wide access for storage NAND. The CPLD incorporates 1.8 to 3.3 volt level translators to interface to the NAND.

2.1.4 Memory Card Interface

The EVM supports MMC/SD media cards via the on chip controller.

2.1.5 UART Interface

The internal UART0 on the DM357 device is driven to connector J6. The UART's interface is level shifted and routed to the RS-232 line drivers prior to being brought out to a DB-9 connector, J6.

2.1.6 EMIF Buffer/Decoder Control CPLD

The EMIF buffer and decode functions are implemented with a CPLD. The EVM board incorporates an Altera MAX II EPM240TCG100 device. The device has 2 banks of I/O. One bank is used for +1.8 volt signals. The other bank is for+3.3 volt signals. This allows the device to do level shifting.

The CPLD incorporates the storage NAND level translators and decode interface along with a divide by 8 counter for video synchronization. The CPLD also incorporates various glue logic for the EVM.

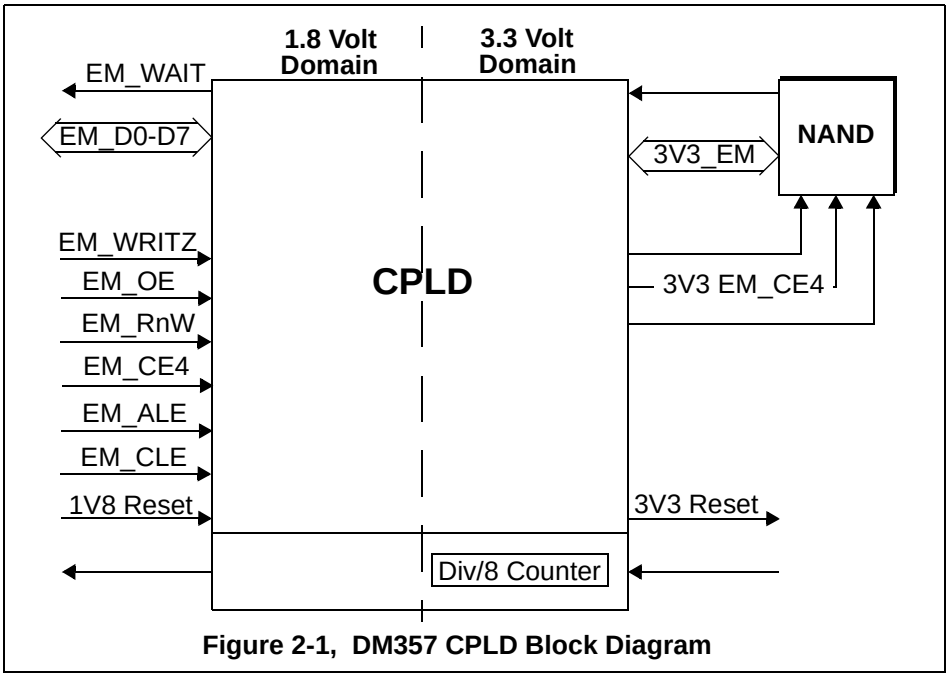

Figure 2-1, DM357 CPLD Block Diagram

2.2 Input Video Port Interfaces

The DM357 EVM supports video capture via the devices internal video ports. A Texas Instruments TVP5146 is used to decode composite video or S-video inputs into the device after being level shifted. J11 is used for the S-video inputs and J12 for the composite inputs on the EVM.

User inputs can be driven via daughter card connector DC4 when the on board level translator is tristate via driving control Capture Enable signal high on DC4.

2.2.1 On Chip Video Output DACs

The DM357 incorporates 1 output DAC to interface to composite video. The DAC is buffered via opamps and driven to connector, J8.

2.2.2 AIC33 Interface

The EVM uses a Texas Instruments TLV320AIC33 stereo codec for input and output of audio signals. The codec samples analog signals on the microphone or line inputs and converts them into digital data so it can be processed by the CPU. When the processor is finished with the data it uses the codec to convert the samples back into analog signals on the line output so the user can hear the output.

The codec communicates using two serial channels, one to control the codec's internal configuration registers and one to send and receive digital audio samples. The I^2C bus is used as the unidirectional control channel. The control channel is generally only used when configuring the codec, it is typically idle when audio data is being transmitted,

The McBSP is used as the bi-directional data channel. All audio data flows through the data channel. Many data formats are supported based on the three variables of sample width, clock signal source and serial data format. The EVM examples generally use a 16-bit sample width with the codec in master mode so it generates the frame sync and bit clocks at the correct sample rate without effort on the processor side.

The codec has a programmable clock from a PLL1705 PLL device. The internal sample rate generator subdivides the default system clock to generate common audio frequencies. The sample rate is set by a codec register. The figure below shows the codec interface on the DM357 EVM.

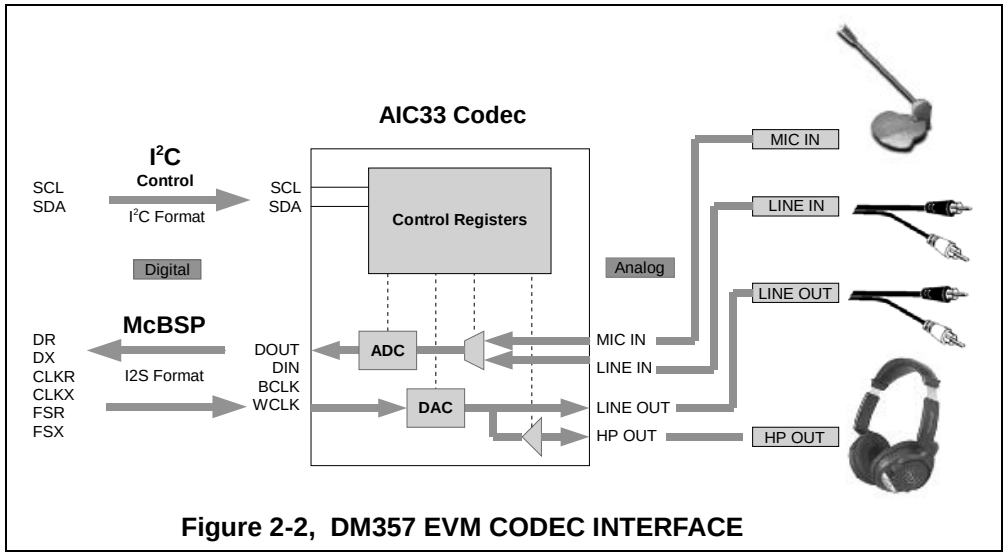

Figure 2-2, DM357 EVM CODEC INTERFACE

2.2.3 Audio PLL/VCXO Circuit/PLL1705 Clock Generator

The DM357 EVM implements a multiple PLL clock generator for creating the Audio clocks for the board.

In streaming video applications the audio and video sequences can lose synchronization. The DM357 uses a VCXO interpolation circuit to incrementally speed up or slow down the STCLK input to allow for this synchronization to remain locked.

The PWM0 and timer inputs on DM357 are used to control this feature. The PWM0 pin drives a PICX100-27W Voltage Controlled Oscillator which is divided by 8 in the CPLD and fed back into the timer input pin.

The STCLK is also a source clock for the PLL1705 programmable PLL device. This device creates the clocks for the AIC33 Codec, daughter card VIDCLK an AUDIOCLK.

The PLL1705 is programmable via an I^2C and Expander U18. Software sequencing on the I/O expander is required to interface correctly to the PLL1708's programmable inputs.

The diagram below is a simplified diagram of this clocking scheme.

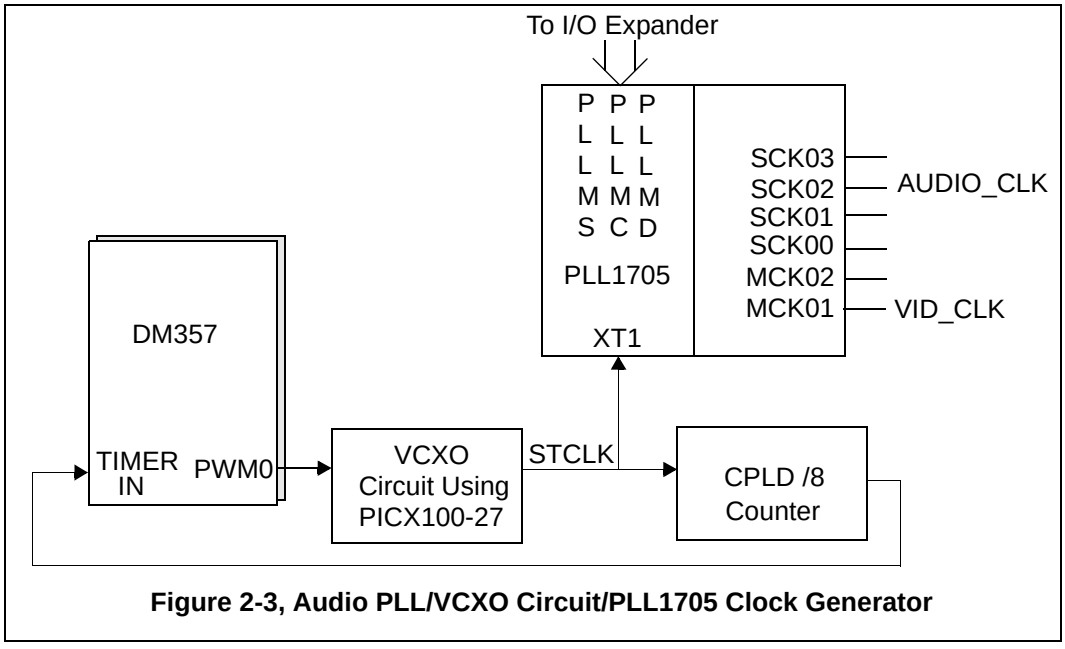

Figure 2-3, Audio PLL/VCXO Circuit/PLL1705 Clock Generator

2.3 Ethernet Interface

The DM357 integrates an ethernet MAC on chip. This interface is routed to the PHY via CBT switches. The EVM uses an Intel LXT971 PHY. The 10/100 Mbit interface is isolated and brought out to a RJ-45 standard ethernet connector, P2. The PHY directly interfaces to the DM357. The ethernet address is stored in the I^2C serial ROM during manufacturing.

The RJ-45 has 2 LEDs integrated into its connector. The LEDs are green and yellow and indicate the status of the ethernet link. The green LED, when on, indicates link and when blinking indicates link activity. The yellow LED, when illuminated, indicates full duplex mode.

When configuring the PHY use the high drive option in the PHY register 26 to compensate for the routing length and extra capacitance of the CBT switches.

2.4 I^2C Interface

The I^2C bus on the DM357 is ideal for interfacing to the control registers of many devices. On the DM357 EVM the I^2C bus is used to configure the video decoder, stereo Codec, I/O expanders, and communicate with the MSP430. An I^2C ROM is also interfaced via the serial bus. The format of the bus is shown in the figure below.

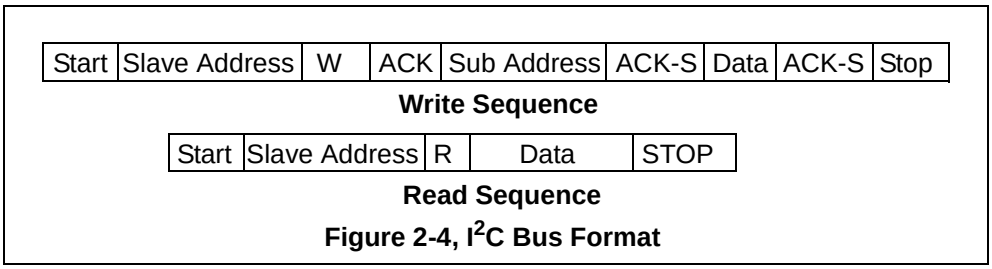

Figure 2-4, I^2C Bus Format

The addresses of the on board peripherals are shown in the table below.

Table 2: I^2C Memory Map

Device	Address	R/W	Function
TVP5146	0x5D	R/W	Capture 1 Decoder
PCF 8574A	0x38	R/W	LEDs
PCF 8574A	0x39	R/W	PLL/User Switch
PCF 8574A	0x3A	R/W	Peripheral Selects
TLV320AIC33	0x1B	R/W	CODEC
24WC256	0x50	R/W	I^2C EEPROM
MSP430	0x23	R/W	LEDs, IR, RTC

2.4.1 I/O Expanders

The DM357 EVM uses three I^2C expanders to handle various bit I/O functions. Each of these is an bit I/O expander, a PCF8574A. At Power Up Reset the expanders are initialized to 0xFF, all ones. The functions for each of the I/O expanders are shown in the tables below.

Table 3: U2, I/O Expander

Pin Number	Function	States
P0	User LED DS8	0 = Turns LED On, 1 = Turns LED Off
P1	User LED DS7	0 = Turns LED On, 1 = Turns LED Off
P2	User LED DS6	0 = Turns LED On, 1 = Turns LED Off
P3	User LED DS5	0 = Turns LED On, 1 = Turns LED Off
P4	User LED DS4	0 = Turns LED On, 1 = Turns LED Off
P5	User LED DS3	0 = Turns LED On, 1 = Turns LED Off
P6	User LED DS2	0 = Turns LED On, 1 = Turns LED Off
P7	User LED DS1	0 = Turns LED On, 1 = Turns LED Off

Table 4: U18, I/O Expander

Pin Number	Function
P0	PLL Program Interface, PLL CSEL Pin
P1	PLL Program Interface, PLL SR Pin
P2	PLL Program Interface, PLL FS1 Pin
P3	PLL Program Interface, PLL FS2 Pin
P4	Spare IO1
P5	Spare IO2
P6	Spare IO3
P7	User DIP Switch *****

* - useful as input only
High Input - Switch in “ON” Position
Low Input - Switch in “OFF” Position

Table 5: U35, I/O Expander

Pin Number	Function	State
P0	Reserved	
P1	VDD IMX Enable	0 = Disables VDDIMX supply
P2	Reserved	
P3	Reserved	
P4	Reserved	
P5	Reserved	
P6	Reserved	
P7	Reserved	

2.4.2 MSP430

The DM357 EVM incorporates infrared remote, real time clock, and some bit I/O in a MSP430 microcontroller. The I^2C interface is used on the DM357 processor to communicate to the MSP430. The MSP430 acts as a slave device on the I^2C bus.

2.5 Daughter Card Interfaces

The EVM provides expansion connectors that can be used to accept plug-in daughter cards. The daughter card allows users to build on their EVM platform to extend its capabilities and provide customer and application specific I/O. The expansion connectors are for all major interfaces including memory, peripherals, and video expansion.

Spectrum Digital produces the THS8200 daughter card (part # 7xxxxx) which plugs onto the connector.

The pin outs for this interface are documented in Section 3.

The memory connector provides access to the CPU's EMIF signals to interface with memories and memory mapped devices.

The video capture port is brought out to the daughter card interface. Four signals are used to disable the on board video peripherals so that they can be used by the expansion connector. The table below indicates the operation of these signals.

Table 6: Daughter Card Video Enable

Signal	State To Enable Daughter Card Use	DM357 Signals Enables
CAPTURE_EN	1	DC4 YI0-YI7 PCLK,VD,HD
McBSP_EN	1	DC3 McBSP
ENET_ENABLE	1	DC2 GIOV33 pins

Other than the buffering, most daughter card signals are not modified on the board.

2.6 DM357 Core CPU Clock

The DM357 EVM uses a 27 Megahertz crystal to generate the input clock. The DM357 has an internal PLL which can multiply the input clock to generate the internal clock. The PLL multiplier is set via software on the DM357 device.

2.7 USB Clock

The DM357 EVM uses a 24 Mhz crystal for the USB II clock generator. The USB controller is completely integrated in the DM357 device.

2.8 Battery

The DM357 EVM incorporates a battery holder to provide backup power to the MSP430's real time clock when the power is not applied to the board. The optional battery should be +3 volt 20 millimeter coin type Lithium single cell.

Some common part numbers for batteries which should operate in the EVM are shown in the table below.

Table 7: Battery Part Numbers

Part Numbers
CR2032
DL2032
BR2032
CR2025
BR2025
CR2016
BR2016
DL2016

These batteries are available from Duracell, Eveready, Panasonic, Ray-O-Vac, Sanyo, Sony, Sieko, Toshiba, Varta, and other battery manufacturers.

Chapter 3

Physical Description

This chapter describes the physical layout of the DM357 EVM and its interfaces.

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3.1 Board Layout

The DM357 EVM is a 6.75 x 10.0 inch (171 x 254 mm.) ten (10) layer printed circuit board which is powered by an external +5 volt only power supply. Figure 3-1 shows the layout of the DM357 EVM.

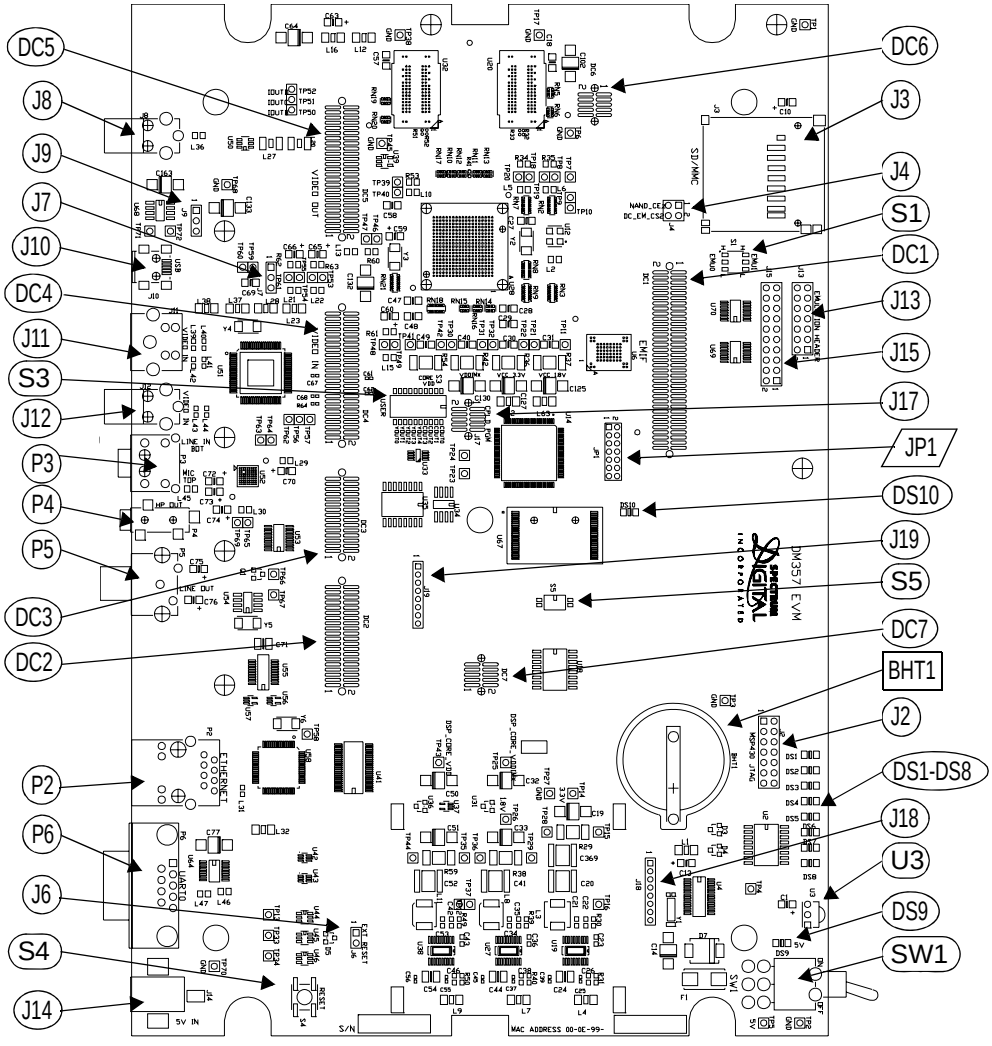

Figure 3-1, DM357 EVM, Interfaces Top Side

3.2 Connectors

The EVM has twenty-nine (29) connectors or interfaces to various peripherals. These connectors are described in the following sections.

Table 1: Connectors

Connector	Size	Function
J2	2 x 7	MSP430 JTAG
J3	24	SD/MMC
J4	2 x 2	EM_CS2 Routing
J6	2	External RESET Input
J7	2	USB Host/Client Termination
J8	RCA	Video Out
J9	1 x 3	USB Capacitance Select
J10	4	MiniAB USB
J11	4 Pin DIN	Composite Video In
J12	RCA	Video In
J13	2 x 7	14 Pin TI Emulation Header
J14	2.5 mm	+5 Volt Input
J15	2 x 10	20 Pin ARM Emulation Header
J17	5 x 2	CPLD Programming Header (Factory Use)
J18	1 x 8, 2mm	MSP430 I/O
J19	1 x 8, 2mm	I/O Header
P2	RJ-45	Ethernet
P3	Dual RCA	Stereo Line In
P4	3.5 mm	Headphone Out
P5	Dual RCA	Stereo Line Out
P6	9	RS-232 UART
DC1	2 x 35	EMIF Expansion
DC2	2 x 20	EMAC/GIO Expansion
DC3	2 x 15	McBSP/SPI Expansion
DC4	2 x 25	Video Input Expansion
DC5	2 x 25	Video Output Expansion
DC6	2 x 5	SD Expansion
DC7	2 x 5	Voltage Expansion
U3		IR Interface

3.2.1 J2, MSP430 JTAG Header

The J2, MSP430 JTAG header, is used to provide a programming interface to the MSP430 microcontroller. The pinout for the J2 connector is shown in the table below.

Table 2: J2, MSP430 JTAG Header

Pin #	Signal	Pin #	Signal
1	430_TDO	2	NC
3	430_TDI	4	MSP430_3V3
5	430_TMS	6	NC
7	430_TCK	8	430_TEST/VPP
9	GND	10	NC
11	NC	12	NC
13	NC	14	NC

3.2.2 J3, SD/MMC Connector

The J3 SD/MMC connector is used to provide an interface to a SD/MMC card. The pinout for the J3 connector is shown in the table below.

Table 3: J3, SD/MMC Connector

Pin #	Signal	Pin #	Signal
1	SD_DATA3	2	SD_CMD
3	GND	4	VCC_3.3V
5	SD_CLK	6	GND
7	SD_DATA0	8	SD_DATA1
9	SD_DATA2	10	GND

3.2.3 J4, EM_CS2 Routing Connector

The J4 connector is actually a 4 position jumper that is used to select the type of memory that the EM_CS2 signal is routed to. The EM_CS2 can be routed to either of the two signals shown in the figure below. Only one (1) device can be selected at a time. To reconfigure this signal, power down the EVM, change the jumper, and then power the board back up. Do **NOT** change this jumper with the power on. The pin outs are shown in the table below.

Table 4: J4, EM_CS2 Routing Connector

Pin #	Signal	Pin #	Signal
1	EM_CS2	3	NAND_CEz
2	EM_CS2	4	DC_EM_CS2

The figure below shows the two possible selections.

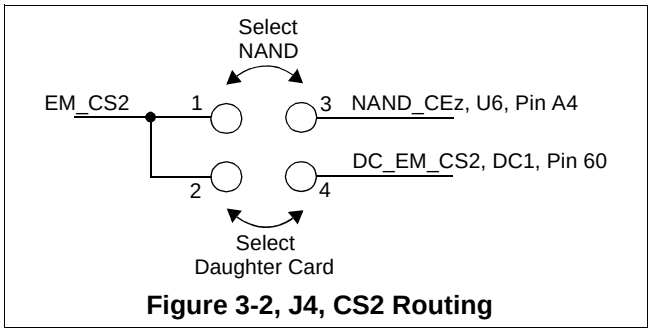

Figure 3-2, J4, CS2 Routing

3.2.4 J6, External RESET Interface

The J6 connector is a 2 position jumper is used to externally reset the board. This connector is unpopulated as shipped from the factory. This circuitry parallels the RESET switch, S4. The figure below represents this connector.

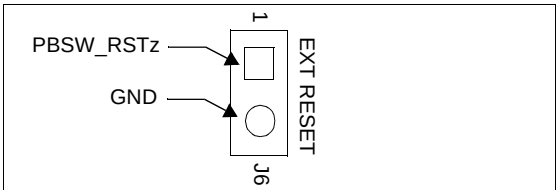

Figure 3-3, J6, External RESET Interface

3.2.5 J7, USB Host/Gadget Termination

The J7 connector is a 3 position jumper that is used to select the termination for the USB host/gadget configuration on USB connector J10. Either the +3.3V (1-2 position) for USB Gadget or Ground (2-3 position) for Host must be selected to properly enable the mode of operation on the DM357 USB controller. To reconfigure this termination, power down the EVM, change the jumper, and then power the board back up. Do **NOT** change this jumper with the power on. The figure below shows the signals on this connector.

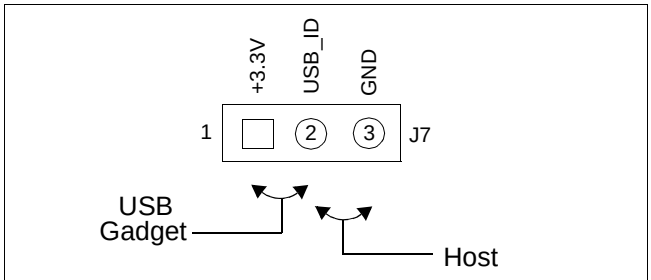

Figure 3-4, J7, USB Host/Gadget Termination

3.2.6 J8, Video Out

The J8 connector is an RCA jack providing 1 DAC output. Do **NOT** plug into these connectors with the power on. This connector is driven by the signal DAC_IOUTA through the op-amp U50.The figure below shows this connector as viewed from the card edge.

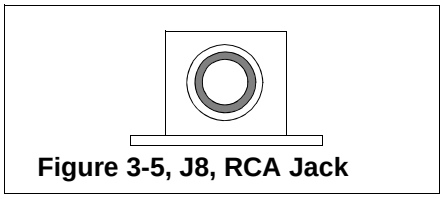

Figure 3-5, J8, RCA Jack

3.2.7 J9, USB Capacitance Select

The J9 jumper is a 3 position jumper header of which only pins 1 and 2 are used. This jumper is used to provide more capacitance when the USB connector is used in the host mode. When the jumper is shorted the extra capacitance is provided. These open and shorted position are shown below.

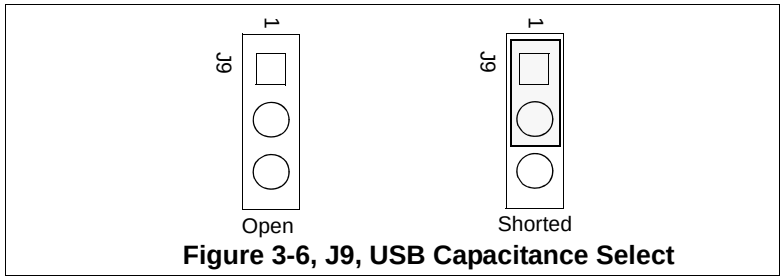

Figure 3-6, J9, USB Capacitance Select

Table 5: J9, USB Capacitance Select

Position	Function
Open	6.8 uF Capacitance
Shorted	106.8 uF Capacitance

3.2.8 J10, MiniAB USB Connector

Connector J10 is a mini A/B USB connector. The pinout for the J10 connector is shown in the table below.

Table 6: J10, MiniAB USB Connector

Pins	Signal
1	USB_VBUS_CONN
2	USB_DM
3	USB_DP
4	USB_ID
5-9	USB_SHIELD/GND

The EVM incorporates the ability to toggle the ID pin on the USB connector via software control. The USB_ID pin on the DM357 controls this function.

For “USB ON The Go” mode remove header J7. This will allow the cable to configure the ID pin on the DM357 processor.

The EVM supplies up to 500 mA of current to the USB_VBUS via a TPS2065D DC/DC converter. This is enabled via the DM357’s DRV_VBUS pin. J9 supplies extra capacitance for host mode operations.

3.2.9 J11, Composite Video In

Connector J11 is a four pin mini-din connector which interfaces to the TVP5146 encoder. This connector brings in a video signal (LUMA) to pin 9 on the TVP5146. Do **NOT** plug into this connector with the power on. The figure below shows this connector as viewed from the card edge.

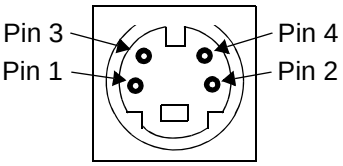

Figure 3-7, J11, Front View, Mini-Din Connector

Table 7: J11, Video In, Mini-Din Connector

Pin #	Signal Name
1	GND
2	GND
3	LUMA
4	Chroma

3.2.10 J12, RCA Jack, Video In

J13 is an RCA jack used as the CVBS/Y input to the TVP5146. The figure below shows this connector as viewed from the card edge.

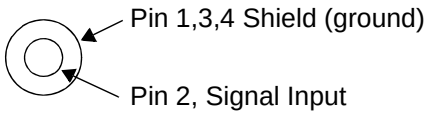

Figure 3-8, J12, Video In RCA Jack

Table 8: J12, Video In RCA Jack

Pin #	Signal Name
1	DEC_GND
2	VI_2_B, U51, Pin 8, TVP5146
3	DEC_GND
2	DEC_GND

3.2.11 J13, 14 Pin TI JTAG Emulation Header

Connector J13 is a 2 x 7 double row male header with pin 6 clipped to serve as a key. This is the standard interface used by JTAG emulators to interface to Texas Instruments processors. The pinout for the connector is shown in the figure below.

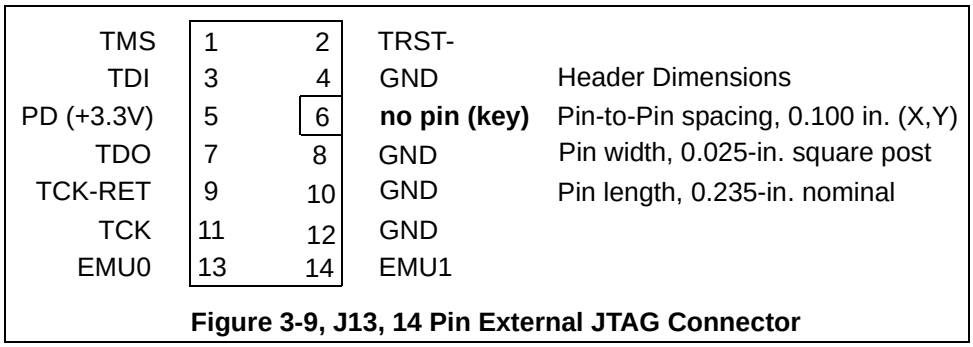

Figure 3-9, J13, 14 Pin External JTAG Connector

The signal names for each pin are shown in the table below.

Table 9: J13, 14 Pin External JTAG Connector

Pin #	Signal Name	Pin #	Signal Name
1	TI TMS	2	TI TRSTn
3	TI TDI	4	GND
5	TI PWR DECT	6	no pin - key
7	TI TDO	8	GND
9	TI TCK RET	10	GND
11	TI TCK	12	GND
13	TI EMU0	14	TI EMU1

* **Note:** EMU0/EMU1 mode must be selected to ICEPICK mode

3.2.12 J14, +5 Volt Input

Connector J14 is the input power connector. This connector brings in +5 volts to the EVM. This is a 2.5mm. jack. Inside of the jack is tied to On/Off power switch SW1. The other side is tied to ground and LED DS9. The figure below shows this connector as viewed from the card edge.

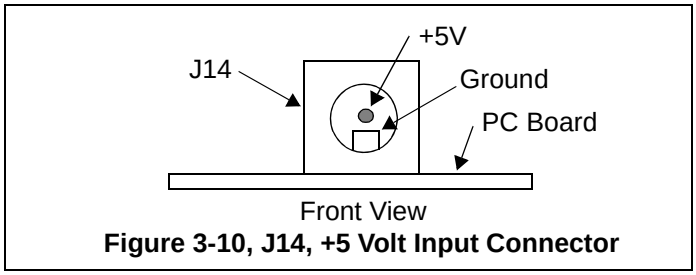

Figure 3-10, J14, +5 Volt Input Connector

3.2.13 J15, 20 Pin ARM JTAG Emulation Header

The J15 emulation header is used to provide an interface to generic ARM9 JTAG emulators. The pinout for this connector is shown in the table below.

Table 10: J15, 20 Pin ARM JTAG Emulation Header

Pin #	Signal	Pin #	Signal
1	VCC_3V3	2	VCC_3V3
3	ARM_TRSTn	4	Ground
5	ARM_TDI	6	Ground
7	ARM_TMS	8	Ground
9	ARM_TCK	10	Ground
11	ARM_TCKRET	12	Ground
13	ARM_TDO	14	Ground
15	ARM_RSTn	16	Ground
17	NC	18	Ground
19	NC	20	Ground

Note: EMU0/EMU1 switch, S1, must be set to ARM mode. This is shown in the figure below. See section 3.5.1 for more details.

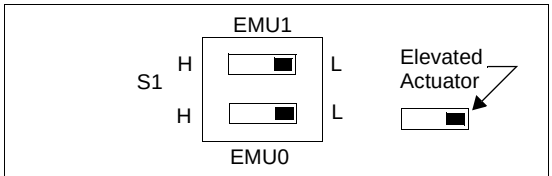

Figure 3-11, S1, EMU0/1 Select Switch
ARM Mode

3.2.14 J17, CPLD Programming Header

Connector J17 is a 10 pin header that provides a programming interface to the FPGA, U14. Do **NOT** plug into this connector with the power on. The table below shows the signals on this connector. This connector is for factory use only. Reprogramming this CPLD affects the functionality of your EVM.

Table 11: J17, CPLD Programming Header

Pin #	Signal	Pin #	Signal
1	ISR_TCK	2	GND
3	ISR_TDO	4	VCC_1.8V
5	ISR_TMS	6	NC
7	NC	8	NC
9	ISR_TDI	10	GND

3.2.15 J18, MSP430 I/O

Connector J18 brings out the I/O lines from the MSP430. These lines are pulled up to +3.3 volts through RN22. The signals on this connector are shown in the table below.

Table 12: J18, MSP430 I/O

Pin #	Signal
1	P2.2/CAOUT/TAO
2	P2.3/CA0/TA1
3	P2.4/CA1/TA2
4	P3.0/STE0/A5
5	P3.1/SIMO0
6	P3.2/SOMI0
7	P3.3/UCLK0
8	P3.7/A7

3.2.16 J19, I2C Bus Expander

Connector J19 brings out the lines from U35, PCF8574A, the remote 8 bit expander for the I2C bus. The signals on this connector are shown in the table below.

Table 13: J18, I2C Bus Expander

Pin #	Signal
1	PIO 0, U35, Pin 4
2	VDDIMX EN, U35, Pin 5
3	PIO 2, U35, Pin 6
4	PIO 3, U35, Pin 7
5	PIO 4, U35, Pin 9
6	PIO 5, U35, Pin 10
7	PIO 6, U35, Pin 11
8	PIO 7, U35, Pin 12

3.2.17 P2, Ethernet

The P2 connector is used to provide an Ethernet interface. P2 integrates the magnetics and standard RJ-45 connector. The two tables below show the signals present on the magnetics interface and the connector side.

Table 14: P2, Magnetics/LEDs Interface Signals

Pin #	Signal	Pin #	Signal
1	TX+, U58, Pin 19	2	TX-, U58, Pin 20
3	RX+, U58, Pin 23	4	TXD-CT, U58, Pin 22
5	RXD-CT, NC	6	RXD-, U58, Pin 24
7	NC1	8	GND
9	LED1+	10	LED1-
11	LED2+	12	LED2-

3.2.18 P3, Dual Stereo Line In

The P3 connector is provides a stereo input (lower) and microphone input (upper) to the TVL320AIC331 on the EVM. A view of the connector from the card edge is shown in the figure below. The signals present on this connector are defined in the following table.

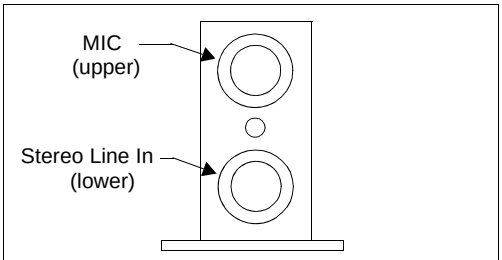

Figure 3-12, P3, Dual Stereo Line In

Table 15: P3, Dual Stereo Line In

Pin #	Signal	Input
1	Isolated Ground	Mic
2	MIC3L/MIC3R, U52, Pins A1,B3	Mic
3	MIC3L/MIC3R, U52, Pins A1,B3	Mic
4	Isolated Ground	Line In
5	LINE1R+/LINE2R+, U52, Pins B4,B7	Line In
6	LINE1L+/LINE2L+, U52, Pins A4,A6	Line In

3.2.19 P4, Headphone Out

The P4 connector is a 3.5 mm. stereo headphone output from the TVL320AIC331ZQE, U52, on the EVM. A view of the connector from the card edge is shown in the figure below.

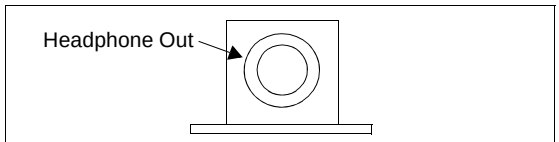

Figure 3-13, P6, Headphone Out Interface

The signals present on this connector are defined in the following table.

Table 16: P4, Headphone Out Interface

Pin #	AIC331 Signal
1	GND
2	HPLOUT, U52, Pin D1
3	HPROUT, U52, Pin G1
4	NC

3.2.20 P5, Stereo Line Out

The P5 connector is a dual output RCA jack bringing audio from the TVL320AIC331 on the EVM. A view of the connector from the card edge is shown in the figure below. The signals present on this connector are defined in the following table.

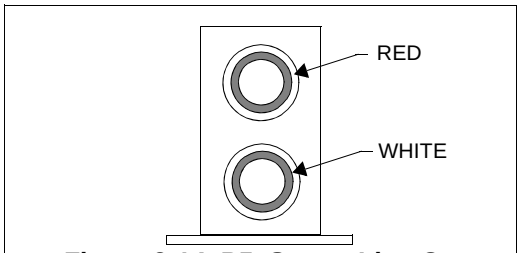

Figure 3-14, P5, Stereo Line Out

Table 17: P5, Stereo Line Out

Pin #	Signal
1	Isolated Ground
2	LEFT_LO+, U52, Pin J4
3	RIGHT_LO+, U52, Pin J6

3.2.21 P6, RS-232 UART

The P6 connector is a 9 pin make D-connector which provides a UART interface to the EVM. This connector interfaces to the MAX 3221 RS-232 line driver (U64) and is located on the top side of the board. A view of the connector from the card edge is shown in the figure below. The signals present on this connector are defined in the following table.

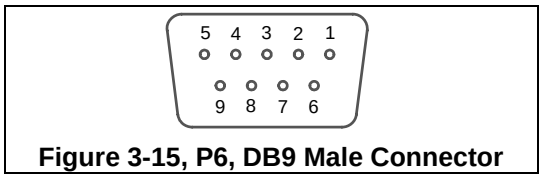

Figure 3-15, P6, DB9 Male Connector

The pin numbers and their corresponding signals are shown in the table below. This corresponds to a standard dual row to DB-9 connector interface used on personal computers.

Table 18: P6, UART Pinout

Pin #	Signal Name	Direction
1	NC	N/A
2	S_A_RXD	In
3	S_A_TXD	Out
4	NC	N/A
5	GND	N/A
6	NC	N/A
7	Connected to pin 8	Out
8	Connected to pin 7	Out
9	NC	N/A
10,11	Earth Ground	N/A

3.2.22 U3, Infrared Interface

U3 is an infrared receiver mounted on the edge of the board. This device interfaces to the MSP430 mircrocontroller. The view of U3 is shown from a board edge view in the figure below.

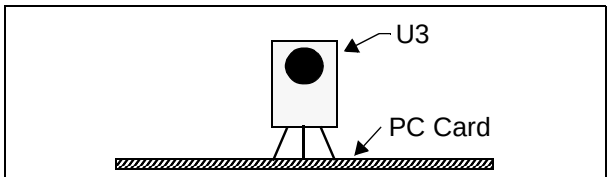

Figure 3-16, U3, IR Interface, Card Edge View

The receiver supports interaction with an Infrared remote control included with your EVM.

Table 19: U3, Infrared Interface

U3 Pin #	MSP430 Signal, Pin #
1	P1.2/TA1, U4, Pin 23
2	GND
3	VCC_3V3

3.3 Daughter Card Connectors

The EVM has seven connectors that are available for daughter card connections. These connectors make many of the signals on the EVM available to be used by external logic. The signals on each of the connectors are described in the following tables. The table below lists the connectors.

Table 20: Daughter Card Connectors

Connector	Size	Function	Schematic Page
DC1	2x35	EMIF	29
DC2	2x20	GIOV33/Ethernet	31
DC3	2x15	SPI, McBSP, I^2C	31
DC4	2x20	Video In	30
DC5	2x25	Video Out	30
DC6	2x5	SD Interface	31
DC7	2x5	Power	35

3.3.1 DC1, EMIF Expansion Connector

Table 21: DC1, EMIF Expansion Connector

Pin #	Signal	Pin #	Signal
1	EM_A21	2	EM_A20
3	EM_A19	4	EM_A18
5	EM_A17	6	EM_A16
7	EM_A15	8	EM_A14
9	GND	10	GND
11	EM_A13	12	EM_A12
13	EM_A11	14	EM_A10
15	EM_A9	16	EM_A8
17	EM_A7	18	EM_A6
19	GND	20	GND
21	EM_A5	22	EM_A4
23	EM_A3	24	CLE_EM_A2
25	ALE_EM_A1	26	EM_A0
27	GND	28	GND
29	GPIO51	30	GPIO52
31	EM_BA1	32	EM_BA0
33	WRITE_WE	34	READ_OE
35	WAIT/BUSY	36	EM_RNW
37	GND	38	GND
39	EM_D15	40	EM_D14
41	EM_D13	42	EM_D12
43	EM_D11	44	EM_D10
45	GND	46	GND
47	EM_D9	48	EM_D8
49	EM_D7	50	EM_D6
51	EM_D5	52	EM_D4
53	GND	54	GND
55	EM_D3	56	EM_D2
57	EM_D1	58	EM_D0
59	EM_CS3	60	DC_EM_CS2
61	1.8V.SYS_RESETz	62	CLKOUT0
63	GND	64	GND
65	VCC_3.3V	66	VCC_3.3V
67	GND	68	GND
69	VCC_5V	70	VCC_1.8V

3.3.2 DC2, EMAC/GIO Connector

Table 22: DC2, EMAC/GIO Connector

Pin #	Signal	Pin #	Signal
1	GND	2	GND
3	GIOV33_0	4	GIOV33_1
5	GIOV33_2	6	GIOV33_3
7	GIOV33_4	8	GIOV33_5
9	GND	10	GND
11	GIOV33_6	12	GIOV33_7
13	GIOV33_8	14	GIOV33_9
15	GIOV33_10	16	GIOV33_11
17	GND	18	GND
19	GIOV33_12	20	GIOV33_13
21	GIOV33_14	22	GIOV33_15
23	GIOV33_16	24	GND
25	GND	26	3V3.SYS_RESETz
27	ENET_ENABLEz	28	GND
29	VCC_1.8V	30	3V3.UART_RXD1
31	VCC_1.8V	32	3V3.UART_TXD1
33	GND	34	GND
35	VCC_3.3V	36	VCC_3.3V
37	VCC_5V	38	VCC_5V
39	GND	40	GND

3.3.3 DC3, McBSP/SPI Expansion

Table 23: DC3, McBSP/SPI Expansion

Pin #	Signal	Pin #	Signal
1	SPI_EN1	2	SPI_EN0
3	SPI_DI	4	SPI_DO
5	SPI_CLK	6	TIMER_IN_DC3
7	GND	8	GND
9	DR	10	DX
11	CLKR	12	CLKX
13	FSR	14	FSX
15	GND	16	GND
17	1.8V.SYS_RESETz	18	1.8V.I2C_CLK
19	McBSP_EN	20	1.8V.I2C_DATA
21	AUDIO_CLK	22	GND
23	GND	24	1.8V_DC3_PCLK
25	VCC_3.3V	26	VCC_3.3V
27	GND	28	GND
29	VCC_5V	30	VCC_1.8V

3.3.4 DC4, Video Input Expansion

Table 24: DC4, Video Input Expansion

Pin #	Signal	Pin #	Signal
1	1.8V.SYS_RESETz	2	CAPTURE_EN
3	GND	4	GND
5	GIO1	6	GIO4
7	GND	8	GND
9	PWM1	10	PWM2
11	GND	12	GND
13	Y10	14	Y11
15	Y12	16	Y13
17	Y14	18	Y15
19	Y16	20	Y15
21	GND	22	GND
23	GND	24	HD
25	PCLK/1V8.DC_PCLK	26	VD
27	GND	28	GND
29	CI0	30	CI1
31	CI2	32	CI3
33	CI4	34	CI5
35	CI6	36	CI7
37	GND	38	GND
39	1V8.I2C_CLK	40	1V8.I2C_DATA
41	VCC_1.8V	42	VCC_1.8V
43	GND	44	GND
45	VCC_3.3V	46	VCC_3.3V
47	GND	48	GND
49	VCC_5V	50	VCC_5V

3.3.5 DC5, Video Output Expansion

Table 25: DC5, Video Output Expansion

Pin #	Signal	Pin #	Signal
1	GIO0	2	GIO2
3	GIO3	4	GIO5
5	GIO6	6	GIO38
7	GND	8	GND
9	COUT0	10	COUT1
11	COUT2	12	COUT3
13	COUT4	14	COUT5
15	COUT6	16	COUT7
17	GND	18	GND
19	VPBECLK/VID_CLK	20	HSYNC
21	GND	22	GND
23	VCLK	24	VSYNC
25	GND	26	GND
27	YOUT0	28	YOUT1
29	YOUT2	30	YOUT3
31	YOUT4	32	YOUT5
33	YOUT6	34	YOUT7
35	GND	36	GND
37	1.8V.I2C_CLK	38	1.8V.SYS_RESETz
39	1.8V.I2C_DATA	40	GND
41	VCC_1.8V	42	VCC_1.8V
43	GND	44	GND
45	VCC_3.3V	46	VCC_3.3V
47	GND	48	GND
49	VCC_5V	50	VCC_5V

3.3.6 DC6, SD Interface Expansion

Table 26: DC6, SD Interface Expansion

Pin #	Signal	Pin #	Signal
1	SD_CLK	2	SD_CMD
3	GND	4	GND
5	SD_DATA0	6	SD_DATA1
7	SD_DATA2	8	SD_DATA3
9	GND	10	GND

3.3.7 DC7, Power Expansion

Table 27: DC7, Power Expansion

Pin #	Signal	Pin #	Signal
1	VDDIMX_EN	2	GND
3	CORE_SUPPLY	4	CORE_SUPPLY
5	GND	6	GND
7	VCC_1.8V	8	VCC_1.8V
9	GND	10	GND

3.4 LEDs

The EVM has ten (10) LEDs which are located on the top side of the board. Eight of these LEDs (DS1-8) are under user control and addressed over the I^2C bus. One LED (DS9) indicates the presence of +5 volts on the board. The remaining LED (DS10) is tied to the CPLD, U14, B2.PIN86, and +3.3 volts. Additional information regarding the LEDs are shown in the table below.

Table 28: LEDs

LED #	Use	Color	Schematic Page
DS1	User Defined	Green	23
DS2	User Defined	Green	23
DS3	User Defined	Green	23
DS4	User Defined	Green	23
DS5	User Defined	Green	23
DS6	User Defined	Green	23
DS7	User Defined	Green	23
DS8	User Defined	Green	23
DS9	+5V	Green	29
DS10	+3.3V, U14, B2.PIN86	Red	14

3.5 Switches

The EVM has five (5) switches. The function of these switches are shown in the table below.

Table 29: Switches

Switch	Function	Type	Schematic Page
S1	EMU0/1 Selection	DIP	28
S3	Boot Configuration Options	DIP	10
S4	RESET	Push button	29
S5	Pull Ups	DIP	14
SW1	Power On/Off	Toggle	29

3.5.1 S1, EMU0/1 Select Switch

S1 is a 2 position DIP switch providing 2 options in selecting the state of the EMU0 and EMU1 pins on the processor. A view of the switch is shown in the figure below. The selection options with this switch are in the table below.

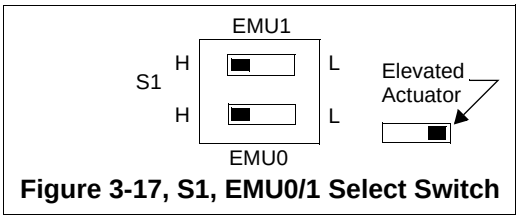

Figure 3-17, S1, EMU0/1 Select Switch

Table 30: S1, EMU0/1 Select

State at Reset EMU0	State at Reset EMU1	Function	TAP Configuration
L	L	Emulation Debug ARM JTAG Enabled (20 pin JTAG connector)	14 bit = (Bypass(6) + ARM9(4) + Bypass(4)
L	H	Not Defined	
H	L	Not Defined	
H	H	TI Emulation Debug * ICE PICK Mode	6 bit = ICE PICK

* is the factory shipped configuration

3.5.2 S3, Processor Configuration/Boot Load Options

S3 is a 10 position DIP switch providing 9 options in selecting the processor configuration and boot load modes. The connections for this switch are shown on page 10 of the schematics in appendix A. A view of the switch is shown in the figure below. The selection options with this switch are in the table below.

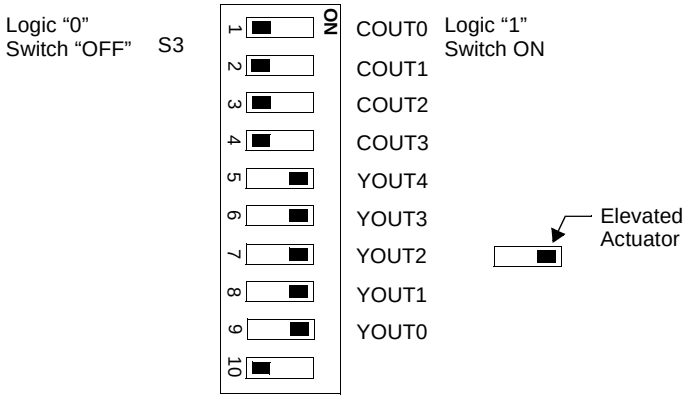

Figure 3-18, S3, Processor Configuration/ Boot Load Options

Table 31: S3, Processor Configuration/Boot Load Options

Position	Name	Function
1	COUT0	0 0 = Boot from ROM (NAND) *****
2	COUT1	0 1 = Boot from AEM IF 1 0 = Boot from ROM (HPI) 1 1 = Boot from ROM (UART)
3	COUT2	Selects AEMIF CS2 Bus width: 0=8 bit *****, 1=16 bit
4	COUT3	Always Low
5	YOUT4	AEAW4
6	YOUT3	AEAW3
7	YOUT2	AEAW2
8	YOUT1	AEAW1
9	YOUT0	AEAW0
10		Composite Video Format

AEAW4:0 configure address pins required to boot. See the tables in the device data sheet for more information. For the DM357 all address active are selected.

3.5.3 S4, RESET

Switch S4 is a push button rest switch that will RESET the processor. This switch is in parallel with J6. The connections for this switch are shown on page 29 of the schematics in appendix A.

3.5.4 S5, User CPLD Option Switch

Switch S5 is a 2 position DIP switch that allows the user to select options on the PIN74 and PIN75 pins of the CPLD, U14. This switch is not used on the DM357 as shipped from the factory. This switch appears on page 14 of the schematics. The diagram below shows which position is associated with each signal.

3.5.5 SW1, Power On/Off

Switch S1 is a toggle switch that provides power to the EVM. The connections for this switch are shown on page 29 of the schematics in appendix A.

3.6 Jumper Block, JP1

The DM357 EVM has 6 position jumper that is not populated. This connector is used for test points on the CPLD internal operations during CPLD debug. The layout of the jumper block is shown below.

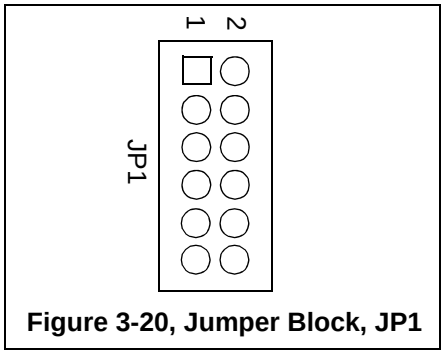

Figure 3-20, Jumper Block, JP1

The signals on each pin are shown in the table below.

Table 32: Jumper Block, JP1

Pin #	Signal	Pin #	Signal
1	U14, PIN92	2	U14, PIN95
3	U14, PIN91	4	U14, PIN96
5	U14, PIN90	6	U14, PIN97
7	U14, PIN89	8	U14, PIN98
9	U14, PIN88	10	U14, PIN99
11	U14, PIN87	12	U14, PIN100

3.8 Test Points

The EVM has 72 test points. All test points appear on the top of the board. The following figure identifies the position of each test point. the next table list each test point and the signal appearing on that test point.

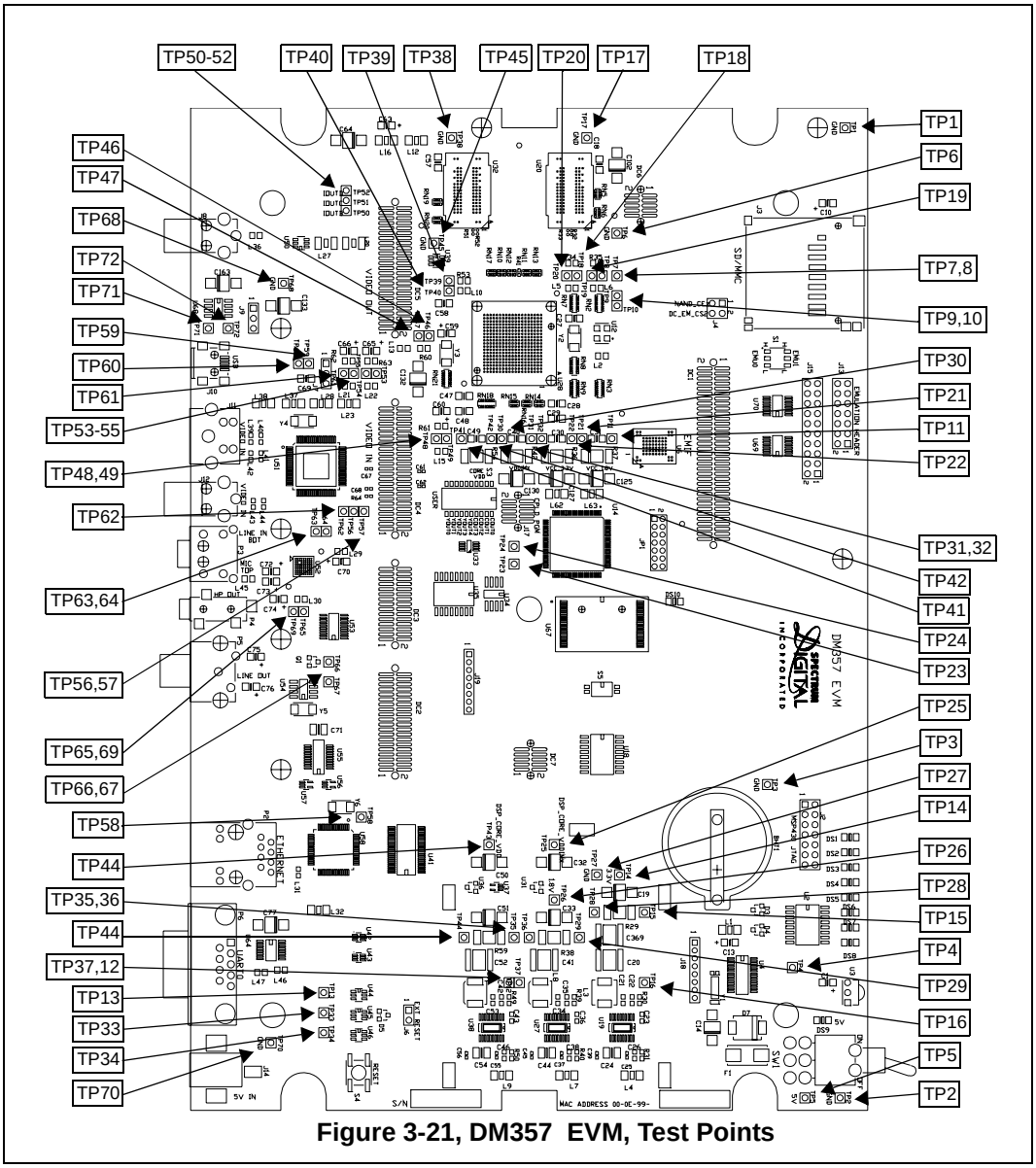

Figure 3-21, DM357 EVM, Test Points

Table 33: DM357 EVM Test Points

TP #	Signal	Page	TP #	Signal	Page
TP1	GND	29	TP37	U27, P4, PWRGD, VCC_5V	30
TP2	GND	29	TP38	GND	4
TP3	GND	29	TP39	U28A,T10, DDR_VDDDLL, 1.8V	4
TP4	U4, P24, P1.3/TA2	24	TP40	VCC_1.8V	4
TP5	VCC_5V	29	TP41	CORE_VDD	9
TP6	GND	4	TP42	U28D, M12, CPU_CORE_VDD	9
TP7	U28A, R8, RSV7	4	TP43	CORE_VDD	30
TP8	U28E, M2, PLLVDD18, VCC_1.8V	8	TP44	CORE_SUPPLY	30
TP9	GND	8	TP45	GND	4
TP10	U28E, L3, RSV6	8	TP46	U28H, H17, USB_VDDA1P8, VCC_1.8V	7
TP11	U28D, T5, CPU_VCC_1.8V, VCC_1.8V	9	TP47	VCC_1.8V	7
TP12	U38, P4, PWRGD, VCC_5V	30	TP48	VCC_3.3V	7
TP13	U44, P1, $\overline{\text{RESET}}$	29	TP49	U28H, J19, USB_VDDA3P3.1, VCC_3.3V	7
TP14	+3.3V	29	TP50	U28G, P18, DAC_IOUT_B	5
TP15	U19, P6, PH1	29	TP51	U28G, R19, DAC_IOUT_C	5
TP16	U19, P4, PWRGD, 3V3_PWR_OK	34	TP52	U28G, T19, RSV45	5
TP17	GND	4	TP53	U28G, R18, VDDA_1P8V, VCC_1.8V	5
TP18	U28E, M3, RSV24, CORE_VDD	8	TP54	VCC_1.8V	5
TP19	VCC_1.8V	8	TP55	U28G, P16, VDDA_1P1V, CORE_VDD	5
TP20	CORE_VDD	8	TP56	U51,Pin 36, AVID/GPIO	20
TP21	VCC_1.8V	9	TP57	U51,Pin 37, GLCO/12CA	20
TP22	U28D, E13, CPU_VCC_3.3V, VCC_3.3V	9	TP58	U58,PIN 64,MDINT	22
TP23	U14, Pin 49, B1.PIN49	14	TP59	J10, Pin 4, USB_ID	17
TP24	U14, Pin 29, B1.PIN29	14	TP60	J10, Pin 1, USB VBUS	17
TP25	CORE_VDDMIX	30	TP61	CORE_VDD	5
TP26	VCC_1.8V	30	TP62	U51,Pin 30, INTREQ	20
TP27	GND	29	TP63	U52, A8, MPF2	22
TP28	VCC_3.3V	29	TP64	U52, A9,MPF3	22
TP29	U27, P6, PH1	30	TP65	U52, J8, GPIO2	22
TP30	CORE_VDDMIX	9	TP66	U28I, C15, PWM0/GIO45, VCC_1.8V	5
TP31	U28DM K11, CPU_CORE_VDDIMX	9	TP67	VIN, U54,PIN 3	5
TP32	VCC_3.3V	9	TP68	GND	29
TP33	U45, P1, $\overline{\text{RESET}}$	29	TP69	U52, J9, GPIO1	22
TP34	U46, P1, $\overline{\text{RESET}}$	29	TP70	GND	29
TP35	U38, P6, PH1	30	TP71	U68, Pin 4, USB.DRVVBUSz	17
TP36	VCC_1.8V	30	TP72	U68, Pin 5, USB.OVER_CURRENT	17

Appendix A

Schematics

This appendix contains the schematics for the DM357 EVM.

REV	DESCRIPTION	DATE	APPROVED
A	Initial schematic ready for layout - Alpha Release	10/15/08	RRP

NOTES, UNLESS OTHERWISE SPECIFIED:

1. RESISTANCE VALUES IN OHMS.
2. CAPACTITANCE VALUES IN MICROFARADS.
3. REFERENCE DESIGNATORS USED:
4. ALL 0.1 uF AND 0.01uF CAPACITORS ARE DECOUPLING CAPS UNLESS OTHERWISE NOTED. THEY ARE SHOWN ON THE PAGE WITH THE INTEGRATED CIRCUITS THEY SHOULD BE PLACED NEAR.
5. OBSERVE THE FOLLOWING LAYOUT NOTES:
6. BOARD PROPERTIES

A. ROUTE TO WITHIN 10% OF MANHATTAN DISTANCE
B1. General layers 50 +/- 5 OHM MATCHED IMPEDANCE
B2. USB layer 90 ohm differential

C. OUTER LAYERS 0.5 OZ CU /W 0.5 OZ AU PLATING
D. INNER LAYERS 1.0 OZ CU
E. FR4 BOARD MATERIAL
F. MINIMUM TRACE WIDTH/SPACING 4 MILS
G. MINIMUM VIA SIZE 10/19 MIL
H. LAYER STACKUP:

1. TOP - SIGNAL ROUTING
2. GROUND PLANE
3. INNER1 - SIGNAL ROUTING
4. VCC3 PLANE (3.3V BOARD)
5. INNER2 - SIGNAL ROUTING
6. INNER3 - SIGNAL ROUTING
7. VCC PLANE 2
8. INNER4 - SIGNAL ROUTING
9. GROUND PLANE
10. BOTTOM - SIGNAL ROUTING

SCHEMATIC CONTENTS

01 DM357 EVM TITLE SHEET
02 DM357 EVM BLOCK DIAGRAM
03 DM357 EMIF INTERFACE
04 DM357 DDR INTERFACE
05 DM357 VIDEO INTERFACE
06 DM357 I/O INTERFACE
07 DM357 USB & SD/MMC/MS CONTROLLER
08 DM357 EMULATION & CLOCKS
09 DM357 POWER PINS
10 DM357 CONFIGURATION CONTROL/BOOT OPTIONS

11 DDR2 MEMORY
12 BOOT NAND FLASH
13 STORAGE NAND FLASH
14 EMIF CPLD MULTIPLEXER
15 SD/MMC CONNECTOR
16 RS232 INTERFACE
17 USB 2.0 INTERFACE
18 ETHERNET INTERFACE
19 TVP5146 LEVEL SHIFTER
20 TVP5416 VIDEO DECODER

21 VIDEO OUT
22 AIC33 AUDIO INTERFACE
23 USER LEDS
24 MSP430 & IR INTERFACE
25 EMIF EXPANSION CONNECTOR
26 VIDEO INPUT/OUTPUT CONNECTORS
27 EMAC/GIO & McBSP/SPI & SD CONNECTORS
28 EMULATION HEADERS
29 POWER SUPPLY (3.3V) & SYSTEM RESET LOGIC
30 POWER SUPPLY (1.8V & CPU_CORE) & EVM POWER CONNECTOR

BASE	I2C ADDRESS TABLE	SHEET
0x50	I2C ROM	6
0x1B	AIC33	22
0x5D	TVP5146	20
0x38	IO EXPANDER 0 (LED)	23
0x39	IO EXPANDER 1 (PLL/USER_SW)	24
0x3A	IO EXPANDER 2 (USB/CD_RESET)	24
0x23	MSP430	24

REVISION STATUS OF SHEETS

REV	A	A	A	A	A	A	A	A	A	A			
SH	21	22	23	24	25	26	27	28	29	30			
REV	A	A	A	A	A	A	A	A	A	A			
SH	11	12	13	14	15	16	17	18	19	20			
REV	A	A	A	A	A	A	A	A	A	A	NEXT ASSY	USED ON	
SH	1	2	3	4	5	6	7	8	9	10	APPLICATION		

		DATE
DWN	R.R.P.	02/17/2005
CHK	T.W.K.	02/17/2005
ENGR	R.R.P.	02/17/2005
ENGR-MGR	R.R.P.	02/17/2005
QA	C.M.D.	03/01/2004
MFG	R.R.P.	02/17/2005
RLSE	R.R.P.	02/17/2005

SPECTRUM DIGITAL INCORPORATED

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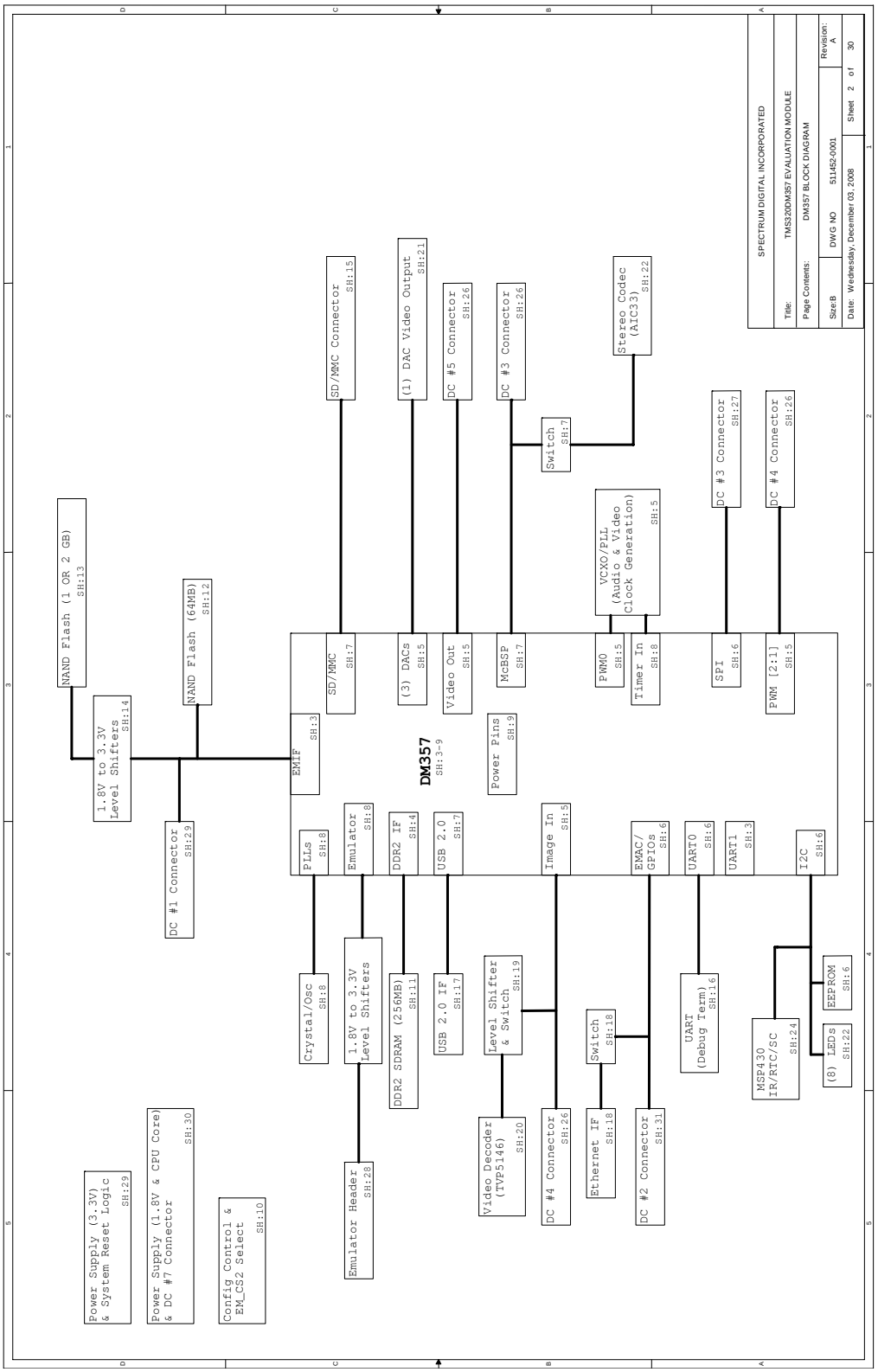
Page Contents:	Title Block	
Size:B	DWG NO 511452-0001	Revision: A
Date: Monday, November 03, 2008		Sheet 1 of 30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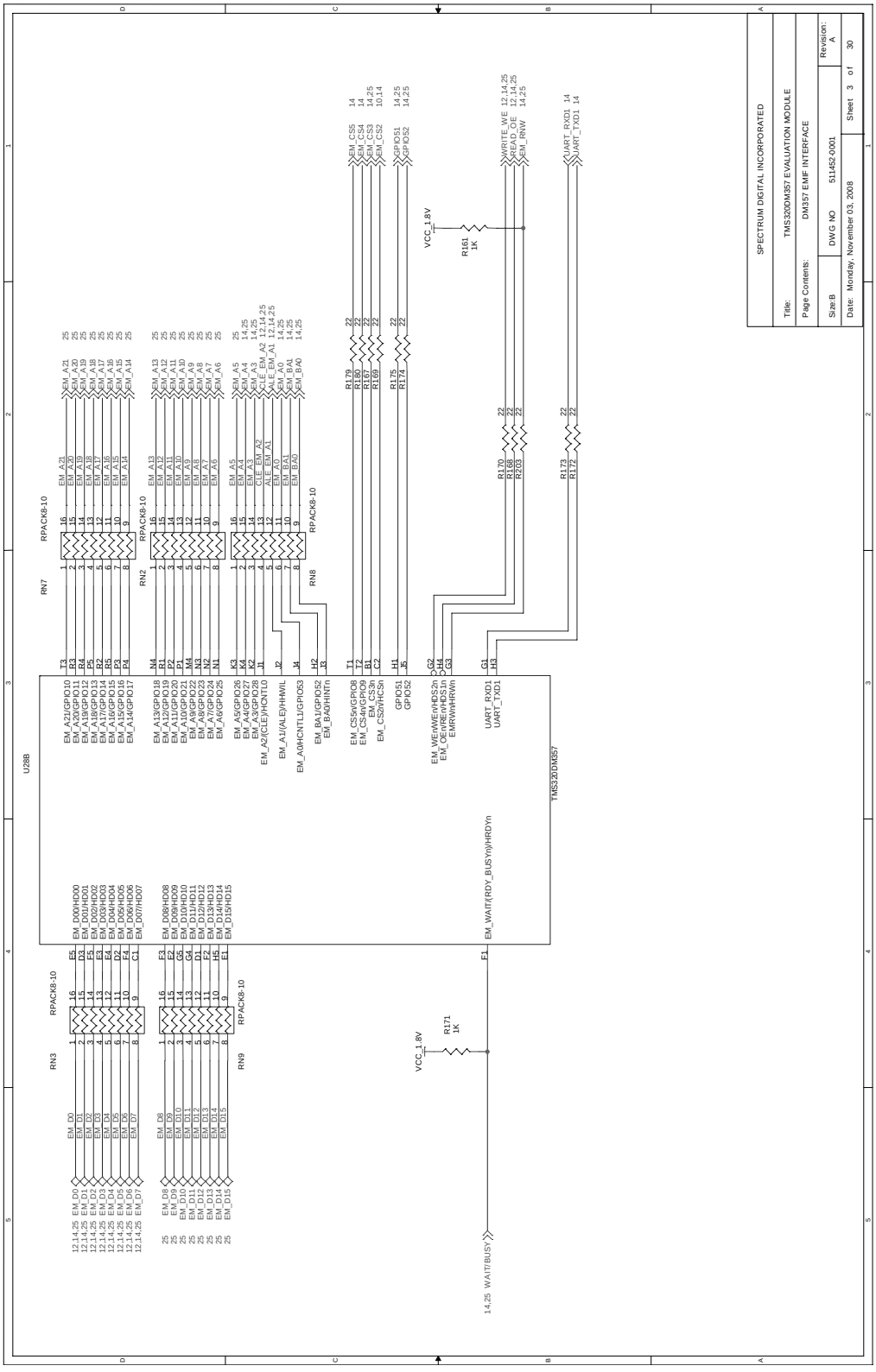
Page Contents: DM357 BLOCK DIAGRAM
Size:B DWG NO 511452-0001 Revision: A
Date: Wednesday, December 03, 2008 Sheet 2 of 30
DM357
SH:3-9
EMIF SH:3
SD/MMC SH:7
(3) DACs SH:5
Video Out SH:5
McBSP SH:7
PWM0 SH:5
Timer In SH:8
SPI SH:6
PWM [2:1] SH:5
PLLs SH:8
Emulator SH:8
DDR2 IF SH:4
USB 2.0 SH:7
Image In SH:5
EMAC/ GPIOs SH:6
UART0 SH:6
UART1 SH:3
I2C SH:6
Power Pins SH:9
SD/MMC Connector SH:15
(1) DAC Video Output SH:21
DC #5 Connector SH:26
DC #3 Connector SH:26
Stereo Codec (AIC33) SH:22
Switch SH:7
VCXO/PLL (Audio & Video Clock Generation) SH:5
DC #3 Connector SH:27
DC #4 Connector SH:26
NAND Flash (1 OR 2 GB) SH:13
1.8V to 3.3V Level Shifters SH:14
NAND Flash (64MB) SH:12
DC #1 Connector SH:29
Crystal/Osc SH:8
1.8V to 3.3V Level Shifters
DDR2 SDRAM (256MB) SH:11
USB 2.0 IF SH:17
Level Shifter & Switch SH:19
Switch SH:18
UART (Debug Term) SH:16
MSP430 IR/RTC/SC SH:24
EEPROM SH:6
(8) LEDs SH:22
Video Decoder (TVP5146) SH:20
DC #4 Connector SH:26
Ethernet IF SH:18
DC #2 Connector SH:31
Emulator Header SH:28
Power Supply (3.3V) & System Reset Logic SH:29
Power Supply (1.8V & CPU Core) & DC #7 Connector SH:30
Config Control & EM_CS2 Select SH:10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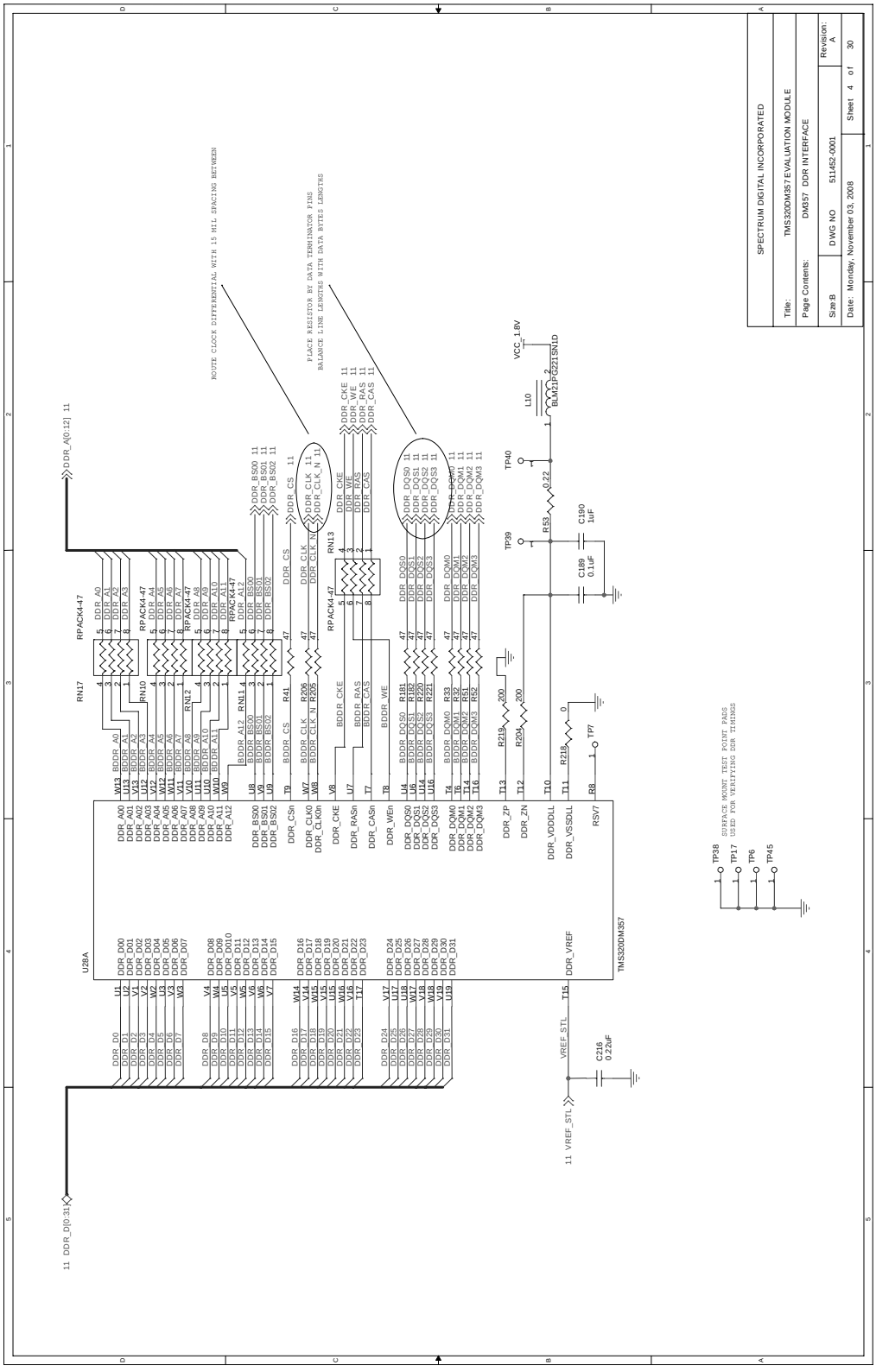
Page Contents: DM357 EMIF INTERFACE
Size: B
DWG NO 511452-0001
Revision: A
Date: Monday, November 03, 2008
Sheet 3 of 30
U28B
TMS320DM357
RN3
RN7
RN2
RN8
RN9
RPACK8-10
R171 1K
R161 1K
R179 R180 R167 R169 R175 R174
R170 R168 R203 R173 R172
VCC_1.8V
EM_D0 EM_D1 EM_D2 EM_D3 EM_D4 EM_D5 EM_D6 EM_D7
EM_D8 EM_D9 EM_D10 EM_D11 EM_D12 EM_D13 EM_D14 EM_D15
EM_D00/HD00 EM_D01/HD01 EM_D02/HD02 EM_D03/HD03 EM_D04/HD04 EM_D05/HD05 EM_D06/HD06 EM_D07/HD07
EM_D08/HD08 EM_D09/HD09 EM_D10/HD10 EM_D11/HD11 EM_D12/HD12 EM_D13/HD13 EM_D14/HD14 EM_D15/HD15
EM_A21/GPIO10 EM_A20/GPIO11 EM_A19/GPIO12 EM_A18/GPIO13 EM_A17/GPIO14 EM_A16/GPIO15 EM_A15/GPIO16 EM_A14/GPIO17
EM_A13/GPIO18 EM_A12/GPIO19 EM_A11/GPIO20 EM_A10/GPIO21 EM_A9/GPIO22 EM_A8/GPIO23 EM_A7/GPIO24 EM_A6/GPIO25
EM_A5/GPIO26 EM_A4/GPIO27 EM_A3/GPIO28 EM_A2/(CLE)/HCNTL0 EM_A1/(ALE)/HHWIL EM_A0/HCNTL1/GPIO53 EM_BA1/GPIO52 EM_BA0/HINTn
EM_CS5v/GPIO8 EM_CS4v/GPIO9 EM_CS3n EM_CS2n/HCSn
EM_WE/WEn/HDS2n EM_OE/REn/HDS1n EM_RW/HRWn
UART_RXD1 UART_TXD1
EM_WAIT/(RDY_BUSYn)/HRDYn
14,25 WAIT/BUSY
EM_CS5 EM_CS4 EM_CS3 EM_CS2
GPIO51 GPIO52
WRITE_WE READ_OE EM_RNW
UART_RXD1 UART_TXD1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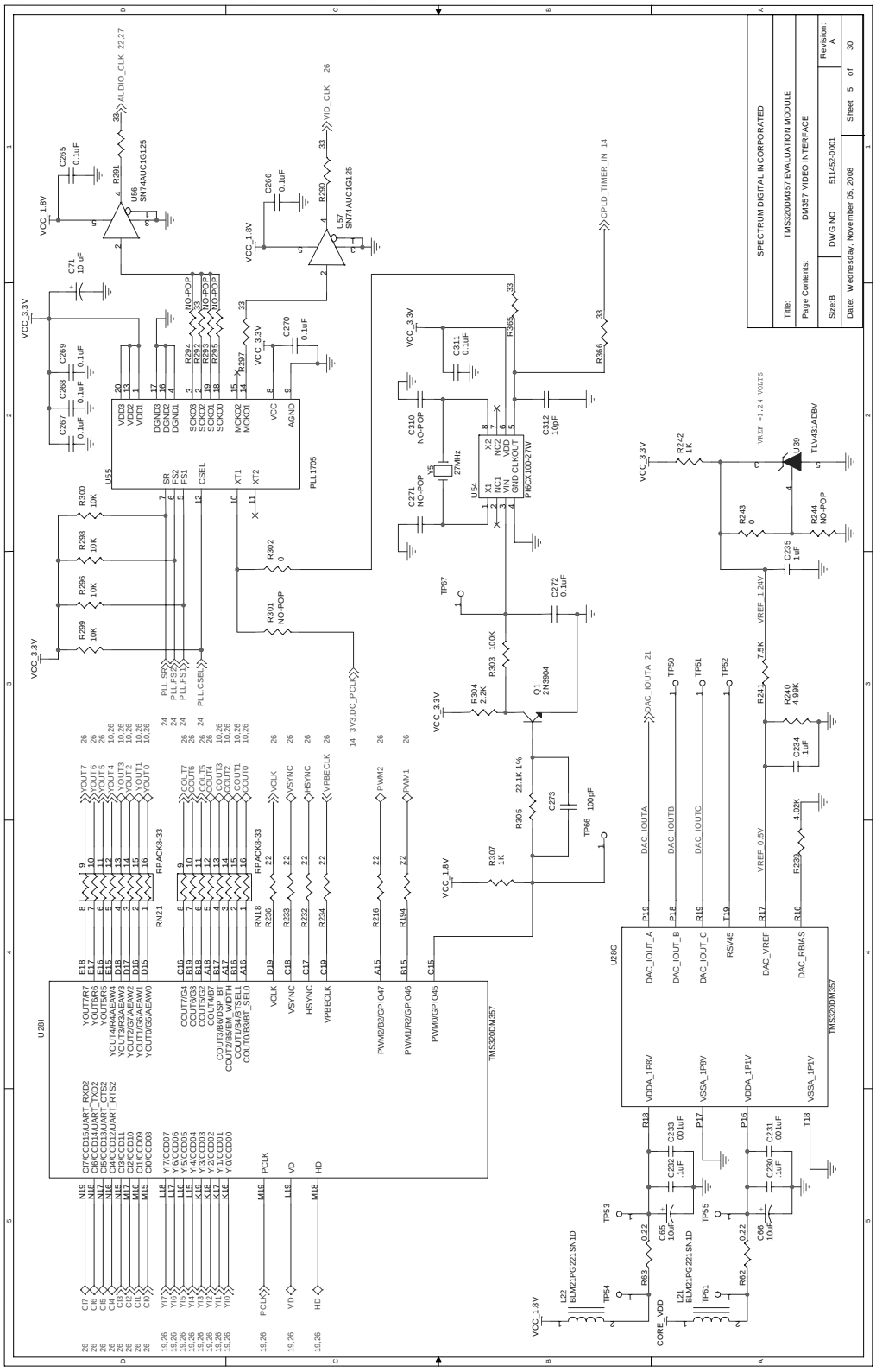
Title: TMS320DM357 EVALUATION MODULE
Page Contents: DM357 DDR INTERFACE
Size: B
DWG NO 511452-0001
Revision: A
Date: Monday, November 03, 2008
Sheet 4 of 30
ROUTE CLOCK DIFFERENTIAL WITH 15 MIL SPACING BETWEEN
PLACE RESISTOR BY DATA TERMINATOR PINS
BALANCE LINE LENGTHS WITH DATA BYTES LENGTHS
U28A
TMS320DM357
RPACK4-47
VCC_1.8V
BLM21B221SN1D
SURFACE MOUNT TEST POINT PADS
USED FOR VERIFYING DDR TIMINGS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Page Contents: DM357 VIDEO INTERFACE
Size:B
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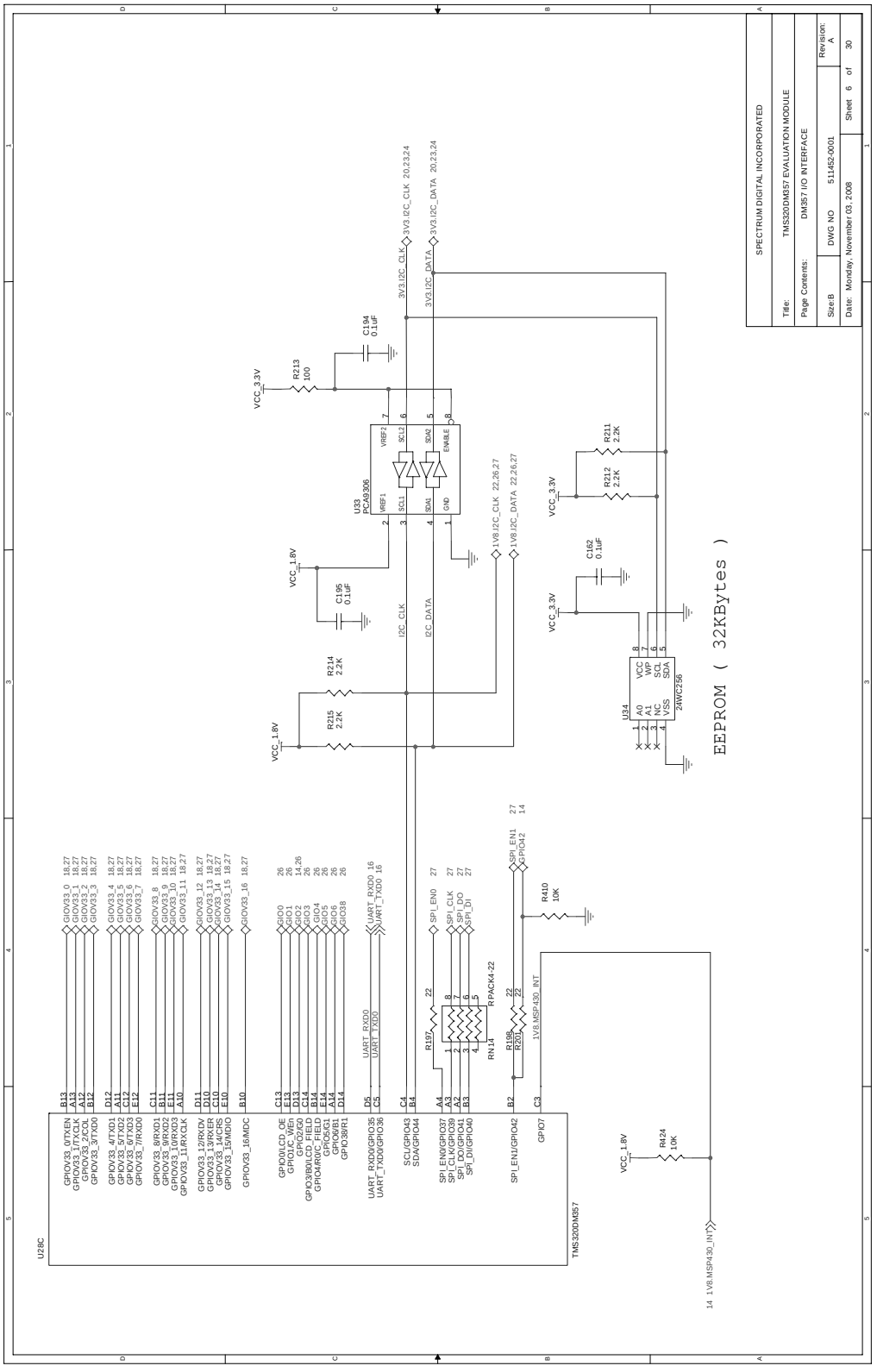
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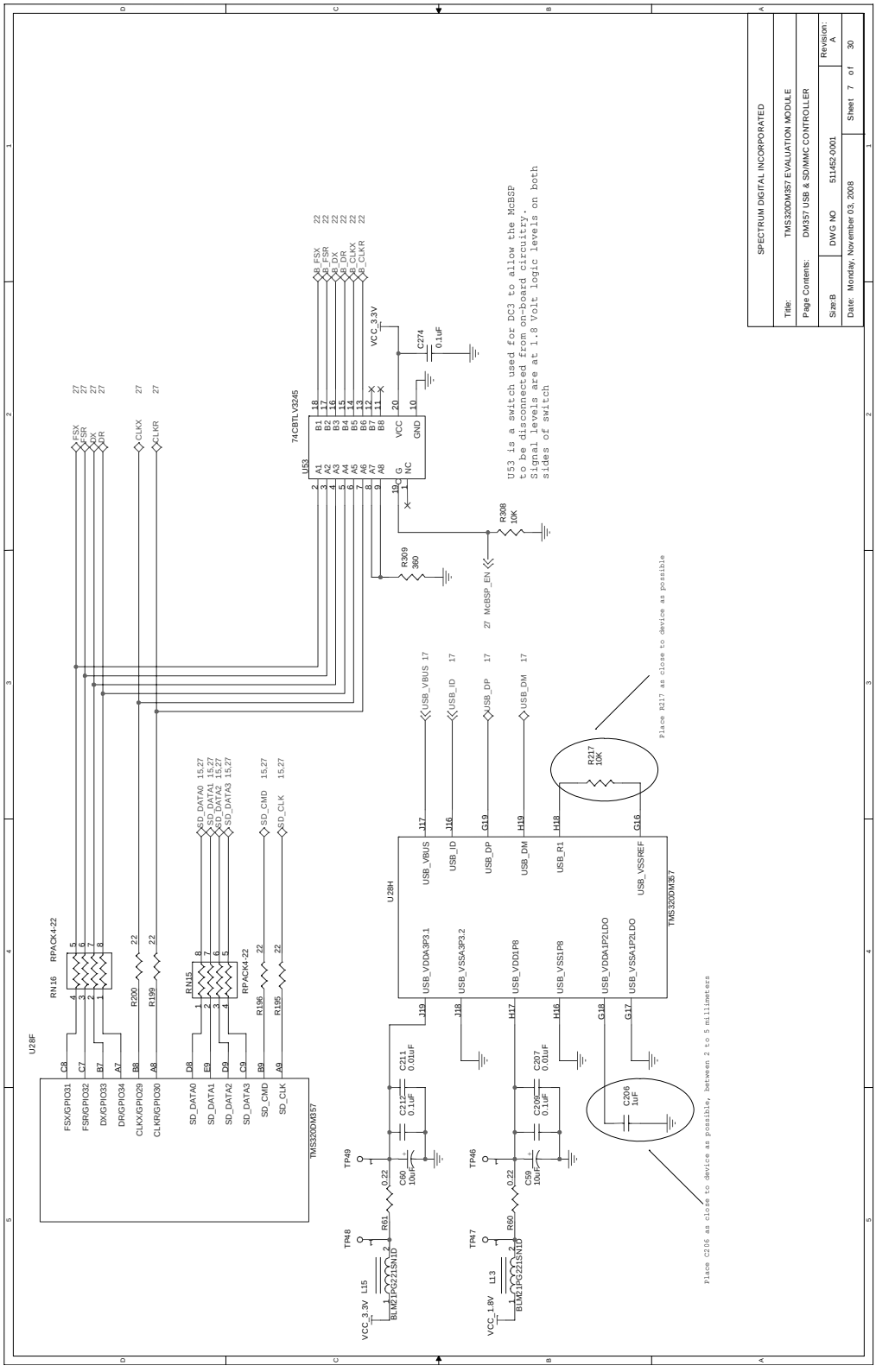
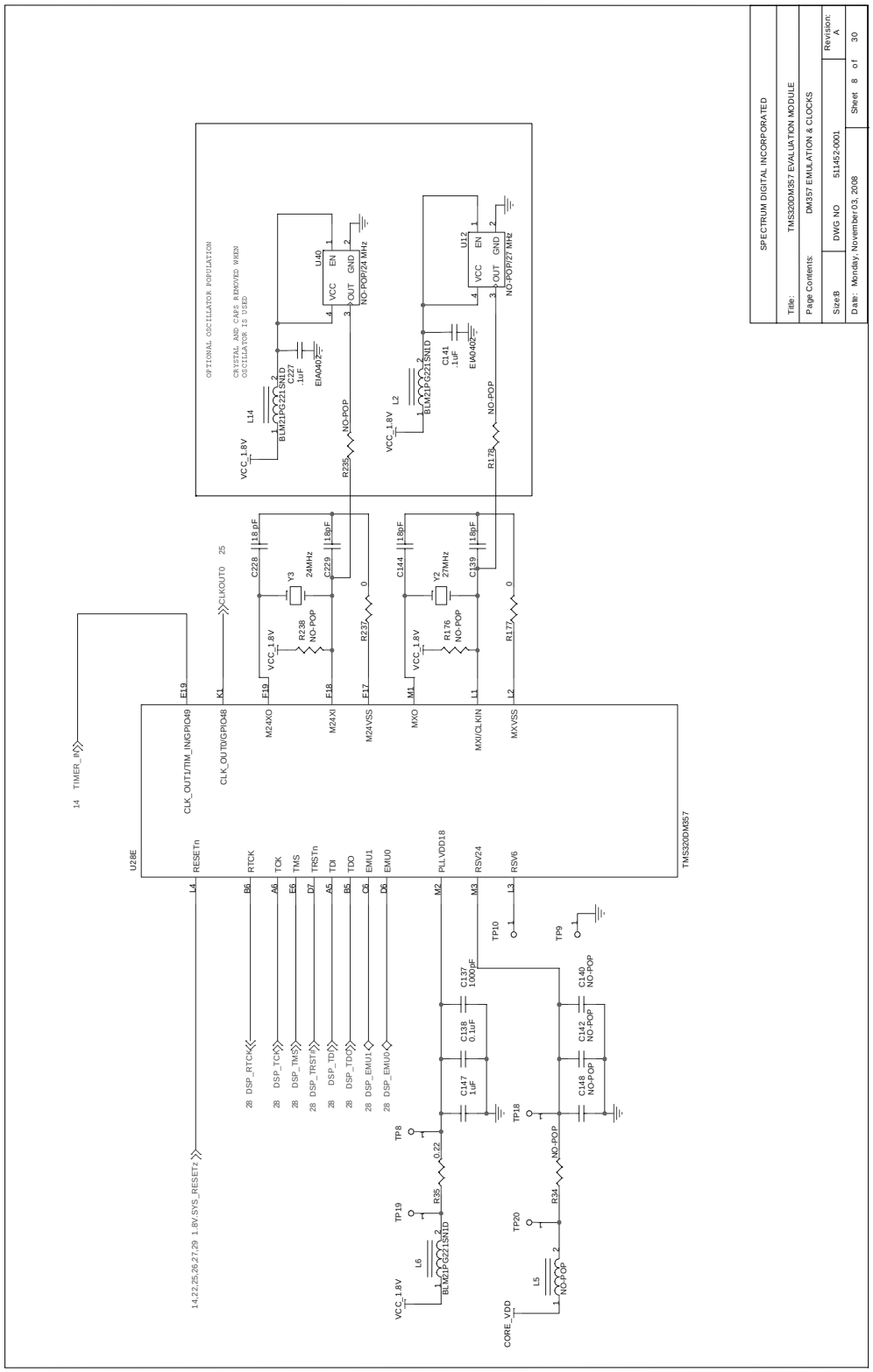
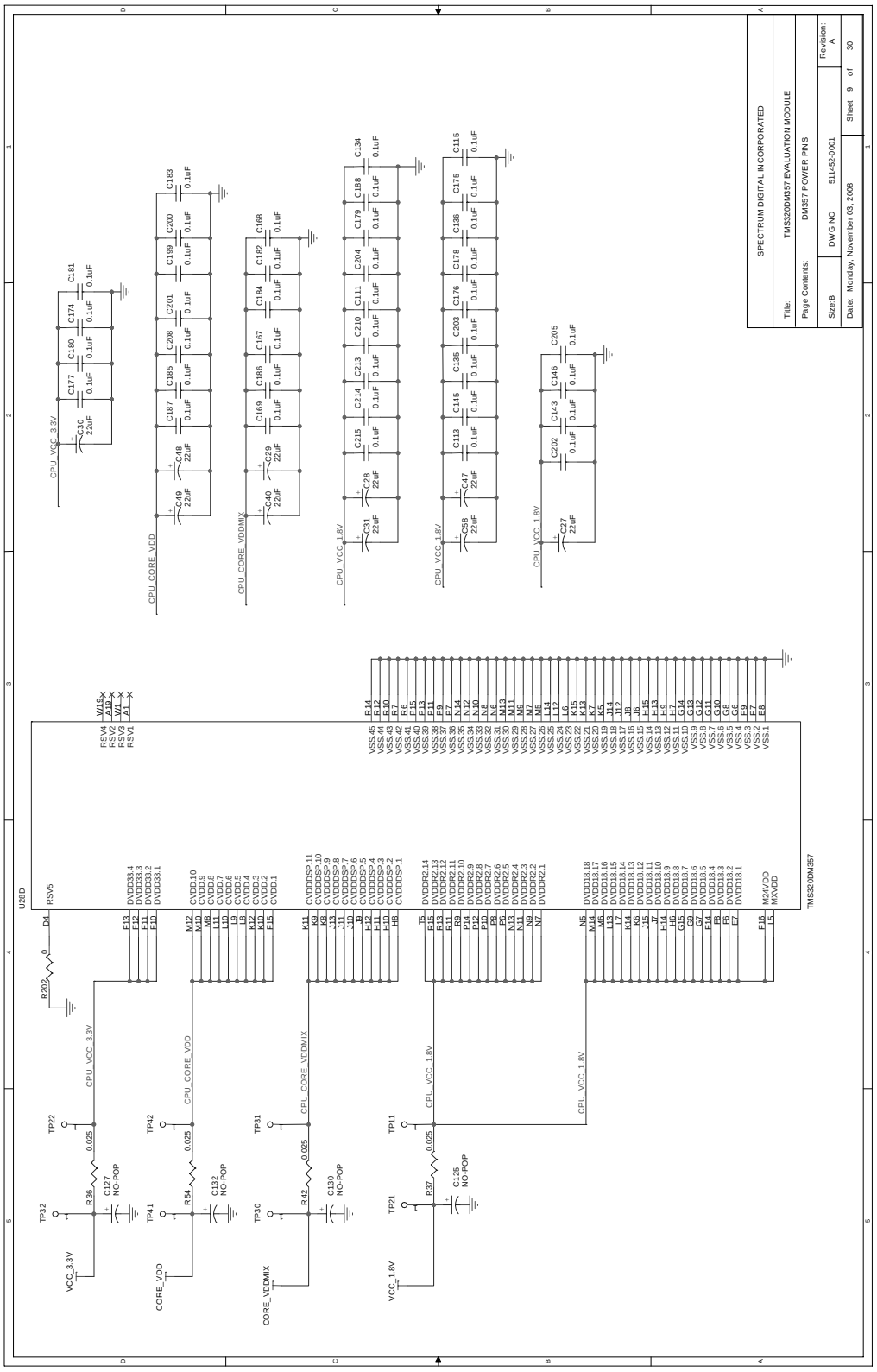
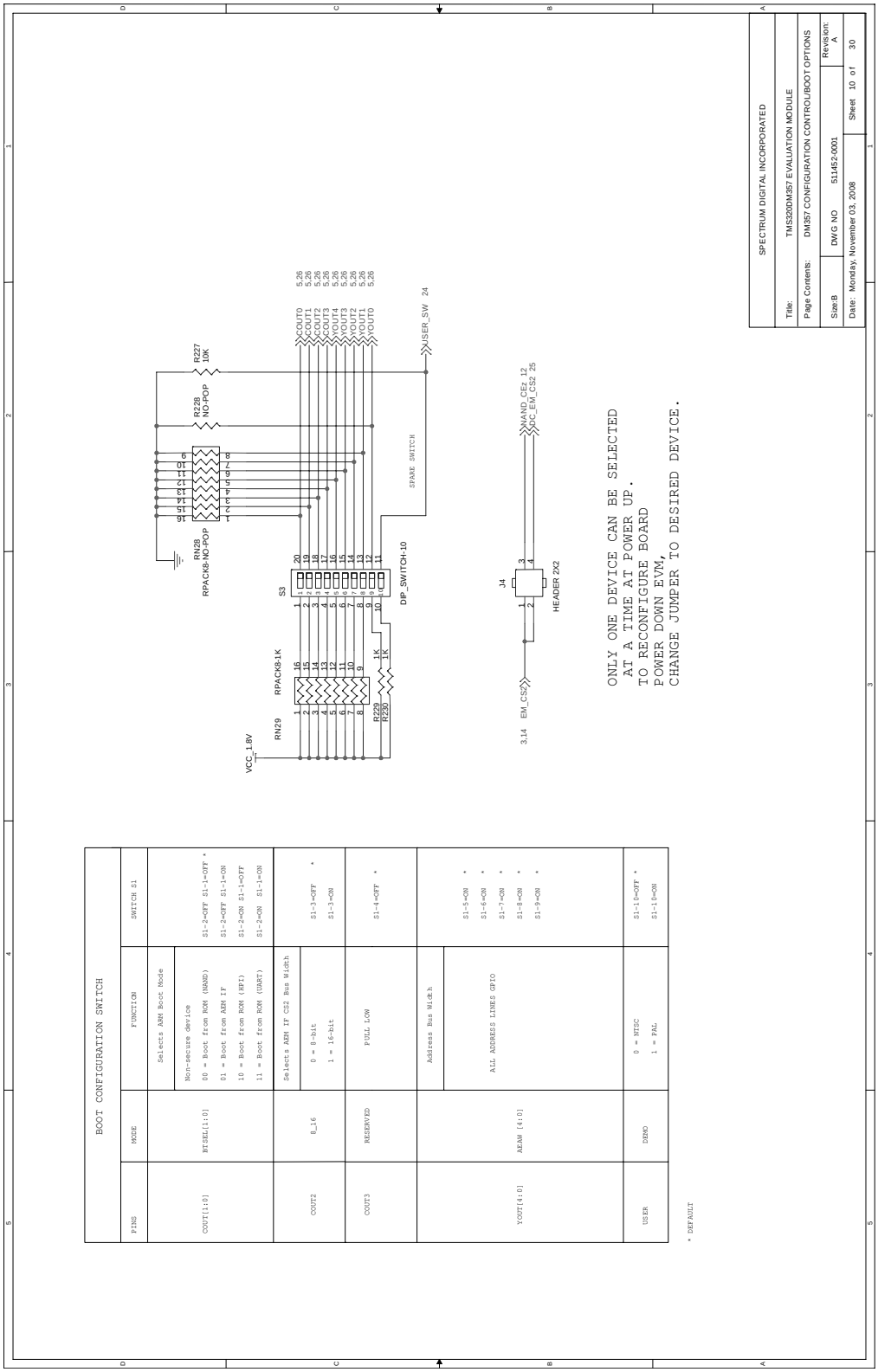
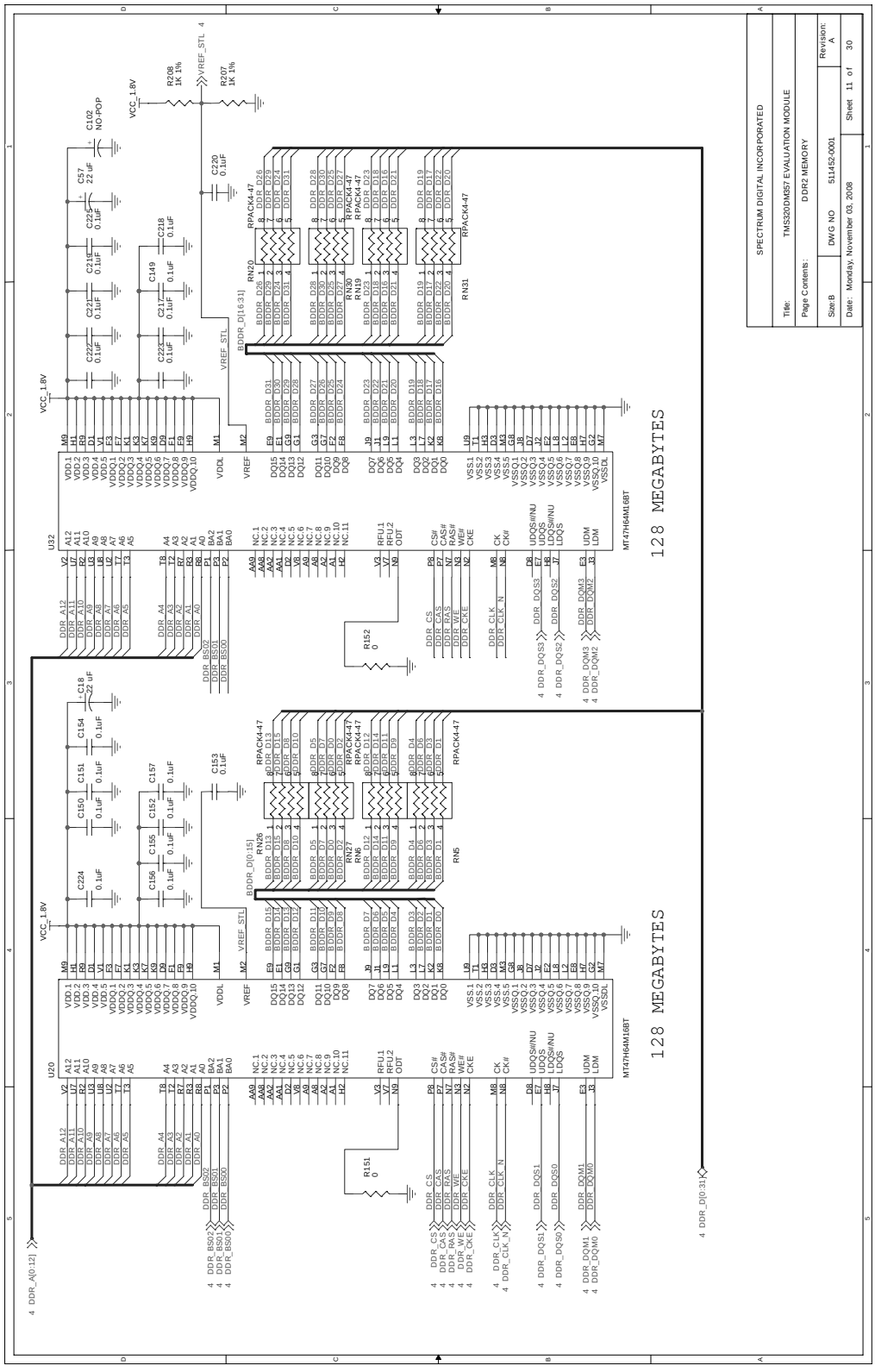
Page Contents: DM357 I/O INTERFACE
Size: B
DWG NO 511452-0001
Revision: A
Date: Monday, November 03, 2008
Sheet 6 of 30
EEPROM (32KBytes)
U28C
TMS320DM357
U33
PCA9306
U34
24WC256
RN14
RPACK4-22
VCC_3.3V
VCC_1.8V
3V3.I2C_CLK 20,23,24
3V3.I2C_DATA 20,23,24
1V8.I2C_CLK 22,26,27
1V8.I2C_DATA 22,26,27
1V8.MSP430_INT
R213 100
C194 0.1uF
C195 0.1uF
R214 2.2K
R215 2.2K
R211 2.2K
R212 2.2K
C162 0.1uF
R410 10K
R424 10K
R197 22
R198 22
R201 22
SPI_EN1 27
GPIO42 14
SPI_EN0 27
SPI_CLK 27
SPI_DO 27
SPI_DI 27
UART_RXD0 16
UART_TXD0 16
GPIO0 26
GPIO1 26
GPIO2 14,26
GPIO3 26
GPIO4 26
GPIO5 26
GPIO6 26
GPIO38 26
GPIOV33_0 18,27
GPIOV33_1 18,27
GPIOV33_2 18,27
GPIOV33_3 18,27
GPIOV33_4 18,27
GPIOV33_5 18,27
GPIOV33_6 18,27
GPIOV33_7 18,27
GPIOV33_8 18,27
GPIOV33_9 18,27
GPIOV33_10 18,27
GPIOV33_11 18,27
GPIOV33_12 18,27
GPIOV33_13 18,27
GPIOV33_14 18,27
GPIOV33_15 18,27
GPIOV33_16 18,27
GPIOV33_0/TXEN
GPIOV33_1/TXCLK
GPIOV33_2/COL
GPIOV33_3/TXD0
GPIOV33_4/TXD1
GPIOV33_5/TXD2
GPIOV33_6/TXD3
GPIOV33_7/RXD0
GPIOV33_8/RXD1
GPIOV33_9/RXD2
GPIOV33_10/RXD3
GPIOV33_11/RXCLK
GPIOV33_12/RXDV
GPIOV33_13/RXER
GPIOV33_14/CRS
GPIOV33_15/MDIO
GPIOV33_16/MDC
GPIO0/LCD_OE
GPIO1/LC_WEn
GPIO2/G0
GPIO3/B0/LCD_FIELD
GPIO4/R0/C_FIELD
GPIO5/G1
GPIO6/B1
GPIO38/R1
UART_RXD0/GPIO35
UART_TXD0/GPIO36
SCL/GPIO43
SDA/GPIO44
SPI_EN0/GPIO37
SPI_CLK/GPIO39
SPI_DO/GPIO41
SPI_DI/GPIO40
SPI_EN1/GPIO42
GPIO7
VCC_1.8V
R424 10K
14 1V8.MSP430_INT

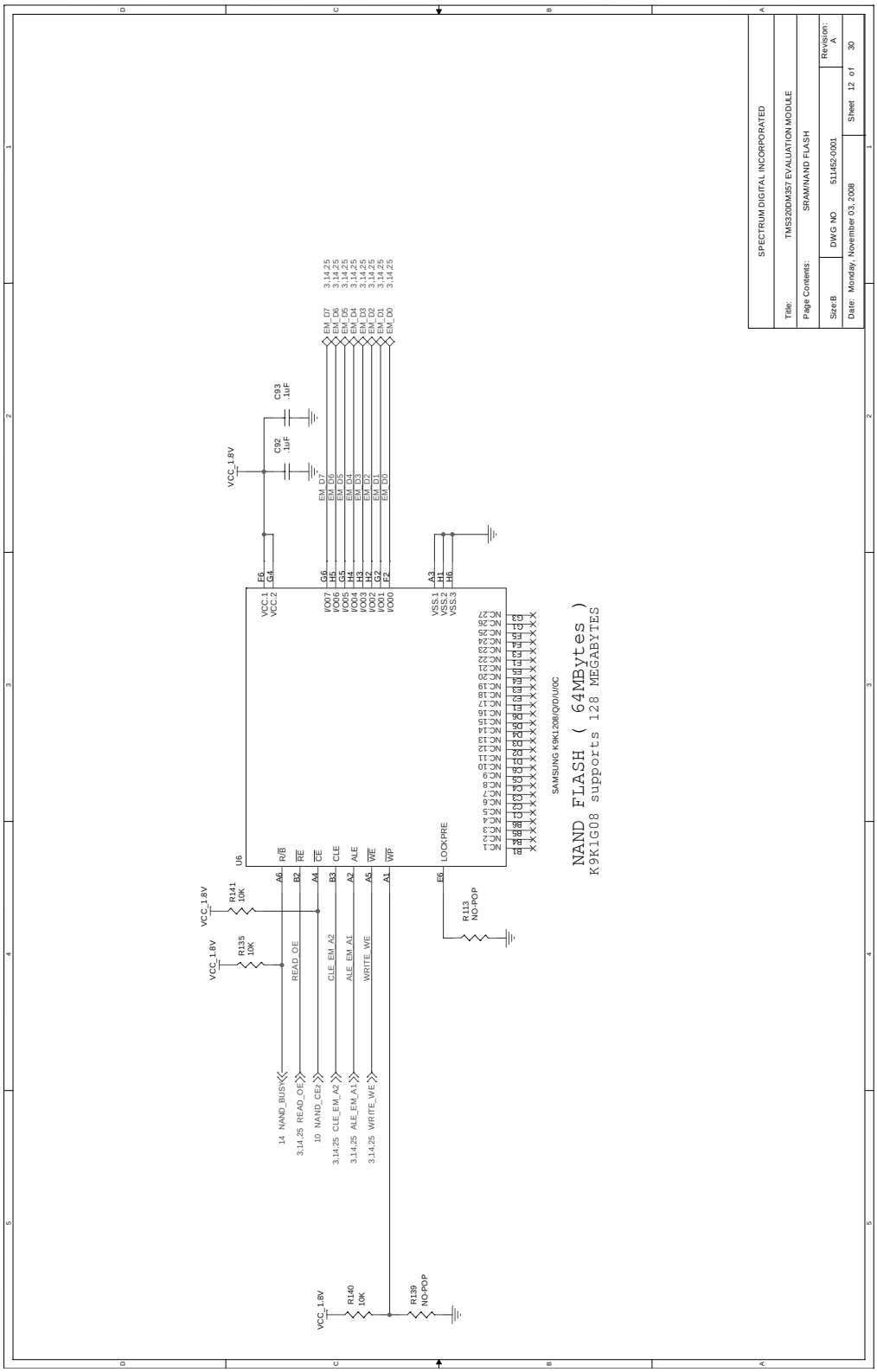

SPECTRUM DIGITAL INCORPORATED
Title: TMS320DM357 EVALUATION MODULE
Page Contents: DM357 USB & SD/MMC CONTROLLER
Size: B
DWG NO 511452-0001
Revision: A
Date: Monday, November 03, 2008
Sheet 7 of 30
U53 is a switch used for DC3 to allow the McBSP to be disconnected from on-board circuitry. Signal levels are at 1.8 Volt logic levels on both sides of switch
74CBTLV3245
TMS320DM357
Place R217 as close to device as possible
Place C206 as close to device as possible, between 2 to 5 millimeters

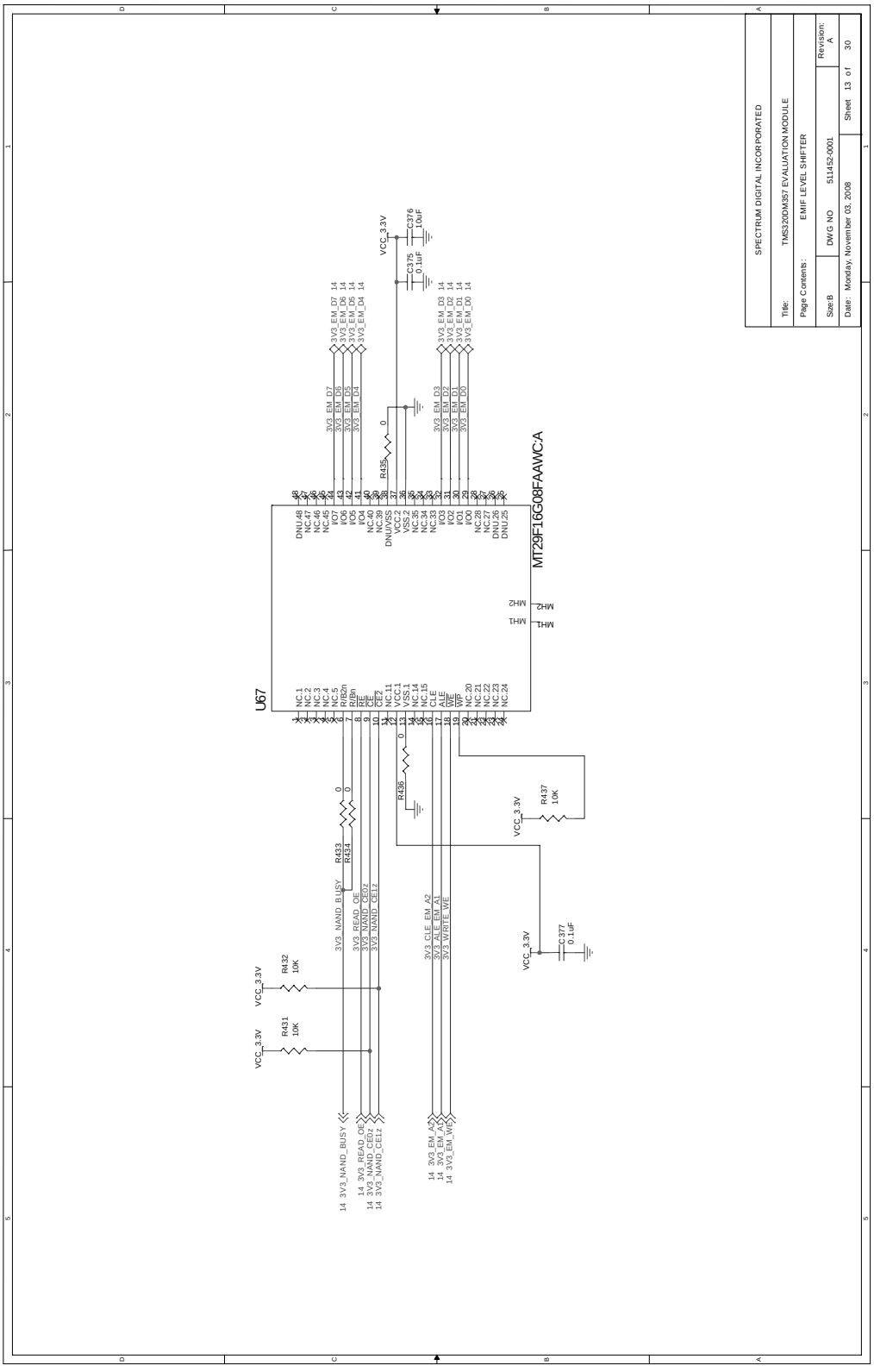

SPECTRUM DIGITAL INCORPORATED
Title: TMS320DM357 EVALUATION MODULE
Page Contents: DM357 EMULATION & CLOCKS
Size:B
DWG NO 511452-0001
Revision: A
Date: Monday, November 03, 2008
Sheet 8 of 30
OPTIONAL OSCILLATOR POPULATION
CRYSTAL AND CAPS REMOVED WHEN OSCILLATOR IS USED
U28E
TMS320DM357
CLK_OUT1/TIM_IN/GPIO49
CLK_OUT0/GPIO48
M24XO
M24XI
M24VSS
MXO
MXI/CLKIN
MXVSS
RESETn
RTCK
TCK
TMS
TRSTn
TDI
TDO
EMU1
EMU0
PLLVDD18
RSV24
RSV6
TIMER_IN
CLKOUT0
SYS_RESET
DSP_RTCK
DSP_TCK
DSP_TMS
DSP_TRSTn
DSP_TDI
DSP_TDO
DSP_EMU1
DSP_EMU0
VCC_1.8V
CORE_VDD
Y3 24MHz
Y2 27MHz
C228 18 pF
C229 18pF
C144 18pF
C139 18pF
R238 NO-POP
R237 0
R176 NO-POP
R177 0
L14 BLM21PG221SN1D
L2 BLM21PG221SN1D
L6 BLM21PG221SN1D
L5 NO-POP
C27 .1uF
C141 .1uF
C137 1000pF
C138 0.1uF
C147 1uF
C140 NO-POP
C142 NO-POP
C148 NO-POP
R235 NO-POP
R178 NO-POP
R35 0.22
R34 NO-POP
U40 VCC EN OUT GND NO-POP/24 MHz
U12 VCC EN OUT GND NO-POP/27 MHz
TP8
TP9
TP10
TP18
TP19
TP20

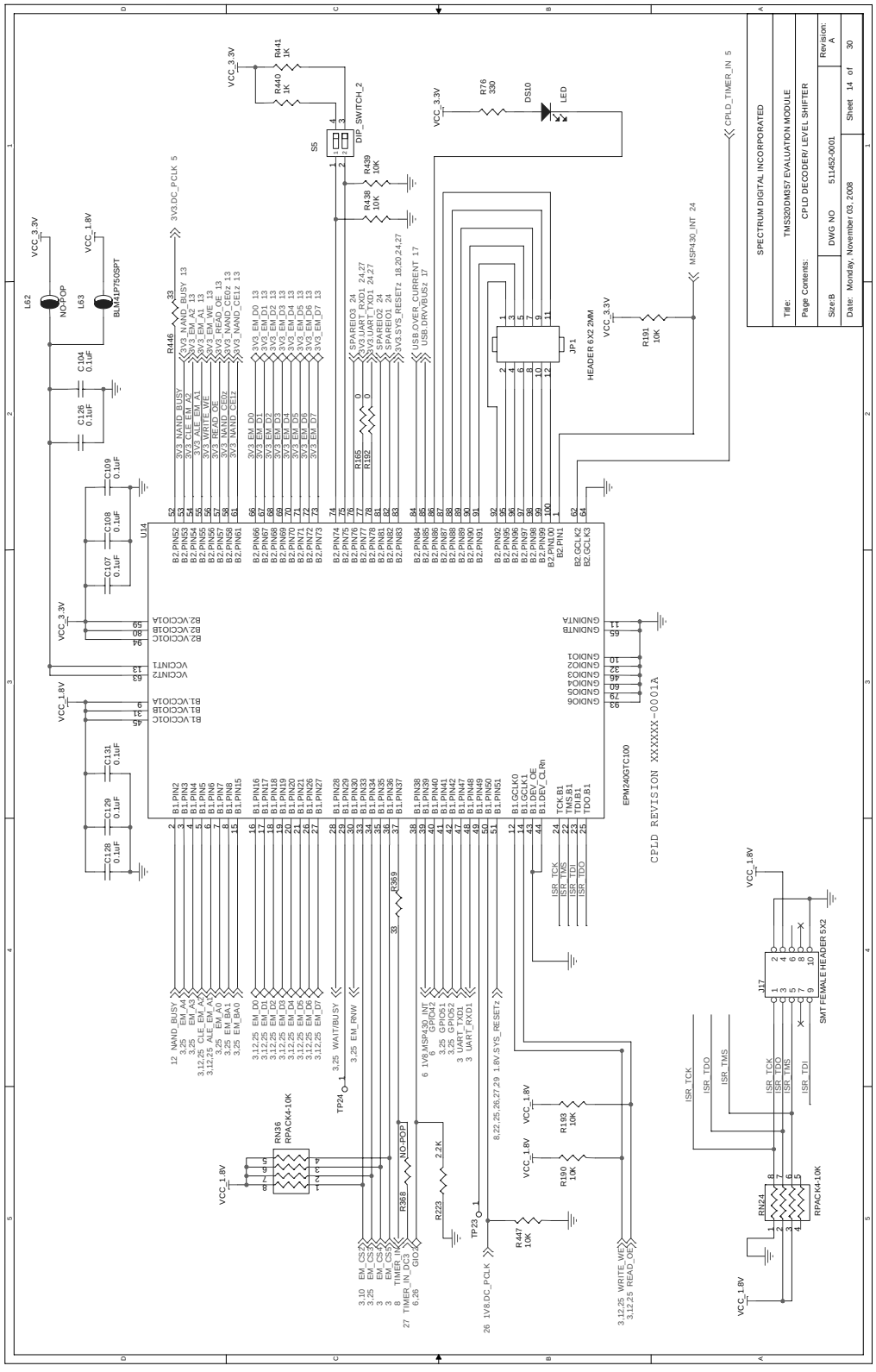

SPECTRUM DIGITAL INCORPORATED
Title: TMS320DM357 EVALUATION MODULE
Page Contents: DM357 POWER PINS
Size:B DWG NO 511452-0001 Revision: A
Date: Monday, November 03, 2008 Sheet 9 of 30
U28D
TMS320DM357
CPU_VCC_3.3V
CPU_CORE_VDD
CPU_CORE_VDDMIX
CPU_VCC_1.8V
VCC_3.3V
CORE_VDD
CORE_VDDMIX
VCC_1.8V
R203 0
R36 0.025
R54 0.025
R42 0.025
R37 0.025
C127 NO-POP
C132 NO-POP
C130 NO-POP
C125 NO-POP
TP22
TP42
TP31
TP11
TP32
TP41
TP30
TP21

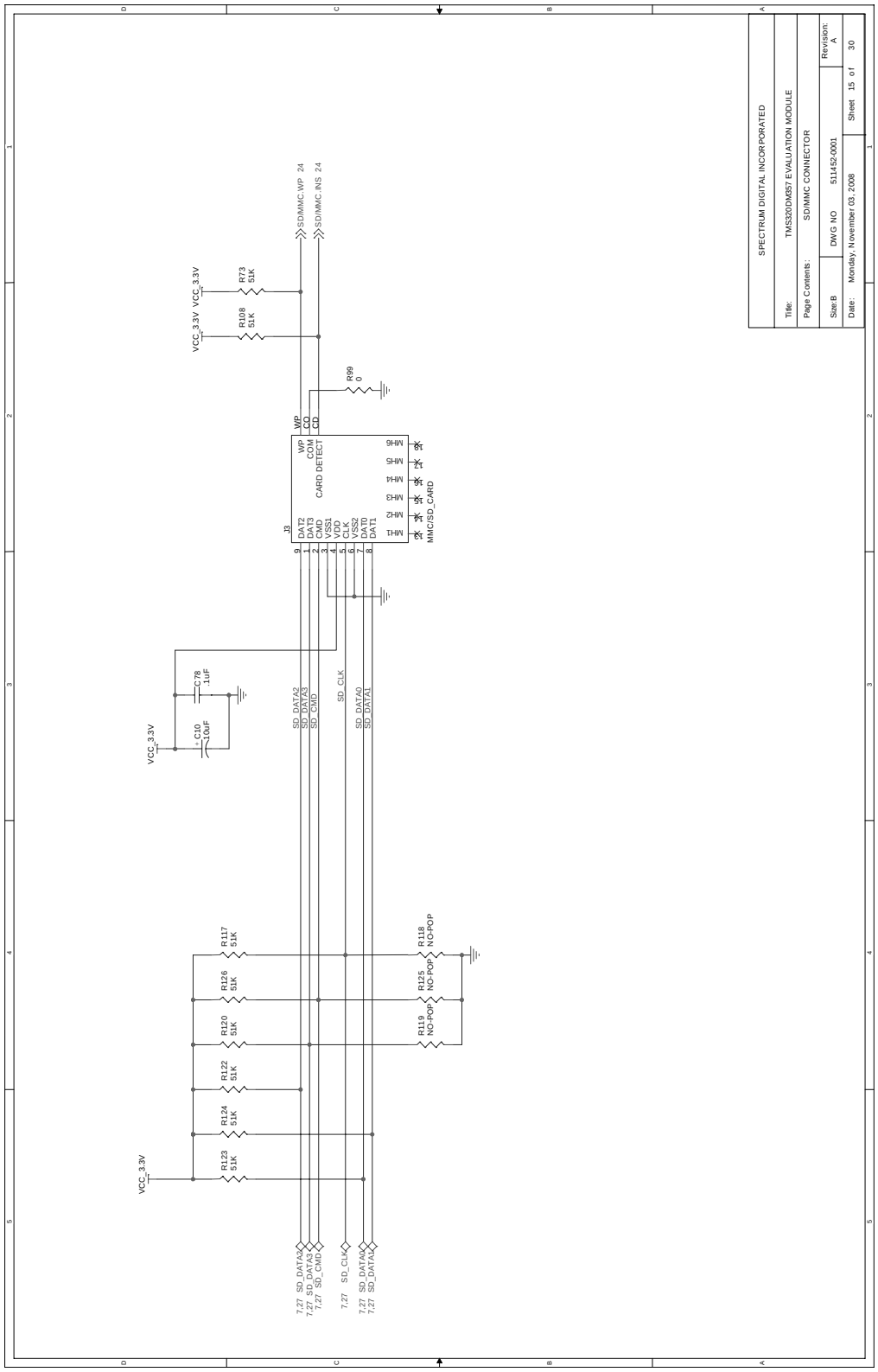

SPECTRUM DIGITAL INCORPORATED
Title: TMS3200M357 EVALUATION MODULE
Page Contents: DM357 CONFIGURATION CONTROL/BOOT OPTIONS
Size:B DWG NO. 511452-0001 Revision: A
Date: Monday, November 03, 2008 Sheet 10 of 30
ONLY ONE DEVICE CAN BE SELECTED
AT A TIME AT POWER UP.
TO RECONFIGURE BOARD
POWER DOWN EVM,
CHANGE JUMPER TO DESIRED DEVICE.
VCC_1.8V
RN29
RPACK8-1K
R229 1K
R230 1K
S3
DIP_SWITCH-10
RN28
RPACK8-NO-POP
R228 NO-POP
R227 10K
USER_SW 24
SPARE SWITCH
COUT0 5,26
COUT1 5,26
COUT2 5,26
COUT3 5,26
YOUT4 5,26
YOUT3 5,26
YOUT2 5,26
YOUT1 5,26
YOUT0 5,26
J4
HEADER 2X2
3,14 EM_CS2
NAND_CE2 12
NOR_EM_CS2 25
BOOT CONFIGURATION SWITCH
PINS
MODE
FUNCTION
SWITCH S1
COUT[1:0]
BTSEL[1:0]
Selects ARM Boot Mode
Non-secure device
00 = Boot from ROM (NAND)
01 = Boot from ARM IF
10 = Boot from ROM (SPI)
11 = Boot from ROM (UART)
S1-2=OFF S1-1=OFF *
S1-2=OFF S1-1=ON
S1-2=ON S1-1=OFF
S1-2=ON S1-1=ON
COUT2
B_16
Selects ARM IF CS2 Bus Width
0 = 8-bit
1 = 16-bit
S1-3=OFF *
S1-3=ON
COUT3
RESERVED
PULL LOW
S1-4=OFF *
YOUT[4:0]
AEAW [4:0]
Address Bus Width
ALL ADDRESS LINES GPIO
S1-5=ON *
S1-6=ON *
S1-7=ON *
S1-8=ON *
S1-9=ON *
USER
DEMO
0 = NTSC
1 = PAL
S1-10=OFF *
S1-10=ON
* DEFAULT

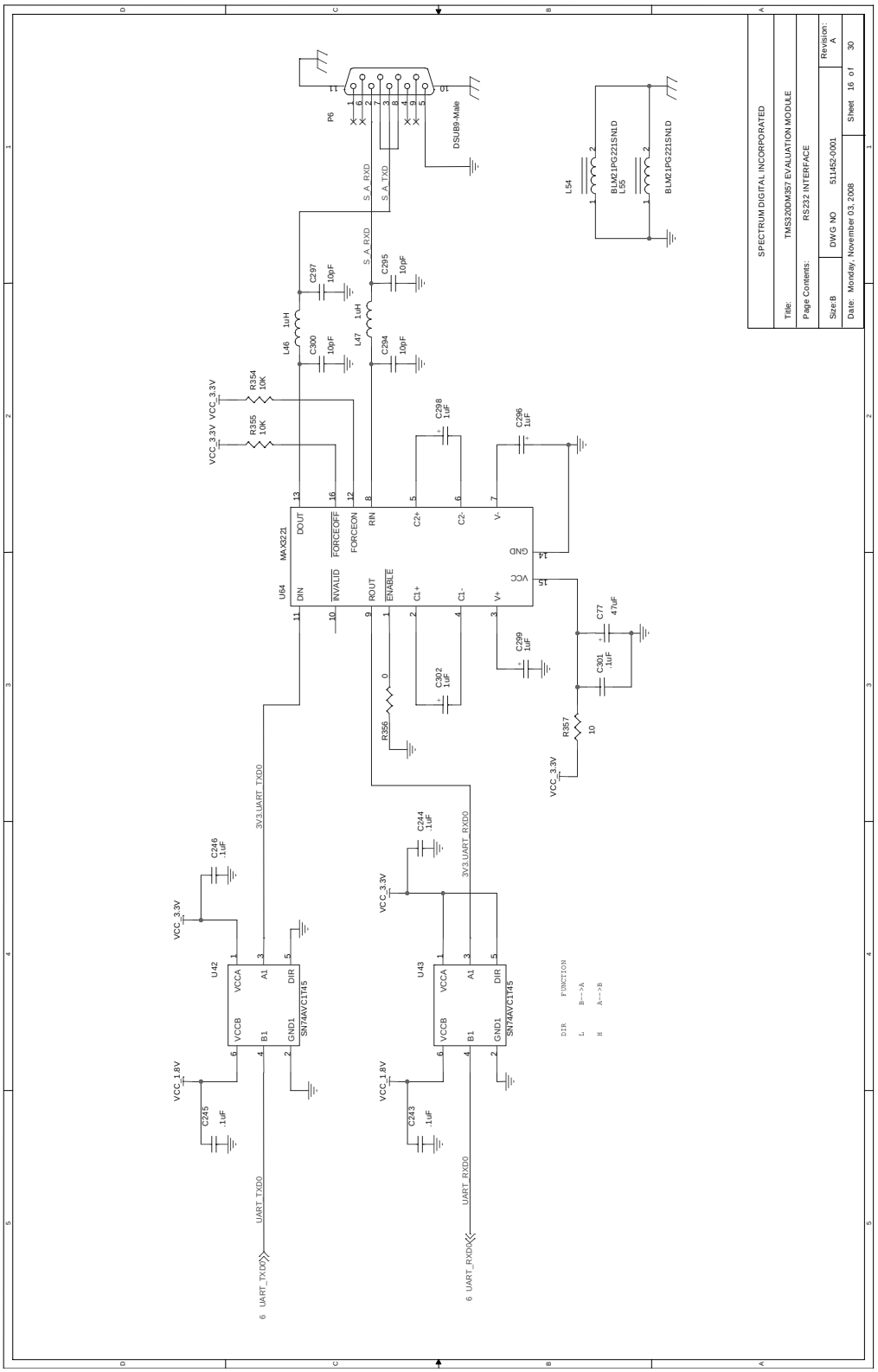

SPECTRUM DIGITAL INCORPORATED
Title: TMS320DM357 EVALUATION MODULE
Page Contents: DDR2 MEMORY
Size: B
DWG NO 511452-0001
Revision: A
Date: Monday, November 03, 2008
Sheet 11 of 30
128 MEGABYTES
128 MEGABYTES
MT47H64M16BT
MT47H64M16BT
U20
U32
VCC_1.8V
VREF_STL
VREF_STL_4
RPACK4-47
RN20
RN31
RN26
RN27
RN5
R151
R152
R208 1K 1%
R207 1K 1%
C102 NO-POP
C57 22 uF
C220 0.1uF
C153 0.1uF
C18 22 uF
C224 0.1uF
C150 0.1uF
C151 0.1uF
C154 0.1uF
C155 0.1uF
C156 0.1uF
C157 0.1uF
C152 0.1uF
C149 0.1uF
C218 0.1uF
C219 0.1uF
C221 0.1uF
C222 0.1uF
C223 0.1uF
C225 0.1uF
C217 0.1uF
C220 0.1uF
4 DDR_A[0:12]
4 DDR_D[0:31]
4 DDR_BS02
4 DDR_BS01
4 DDR_BS00
4 DDR_CS
4 DDR_CAS
4 DDR_RAS
4 DDR_WE
4 DDR_CKE
4 DDR_CLK
4 DDR_CLK_N
4 DDR_DQS1
4 DDR_DQS0
4 DDR_DQM1
4 DDR_DQM0
4 DDR_DQS3
4 DDR_DQS2
4 DDR_DQM3
4 DDR_DQM2

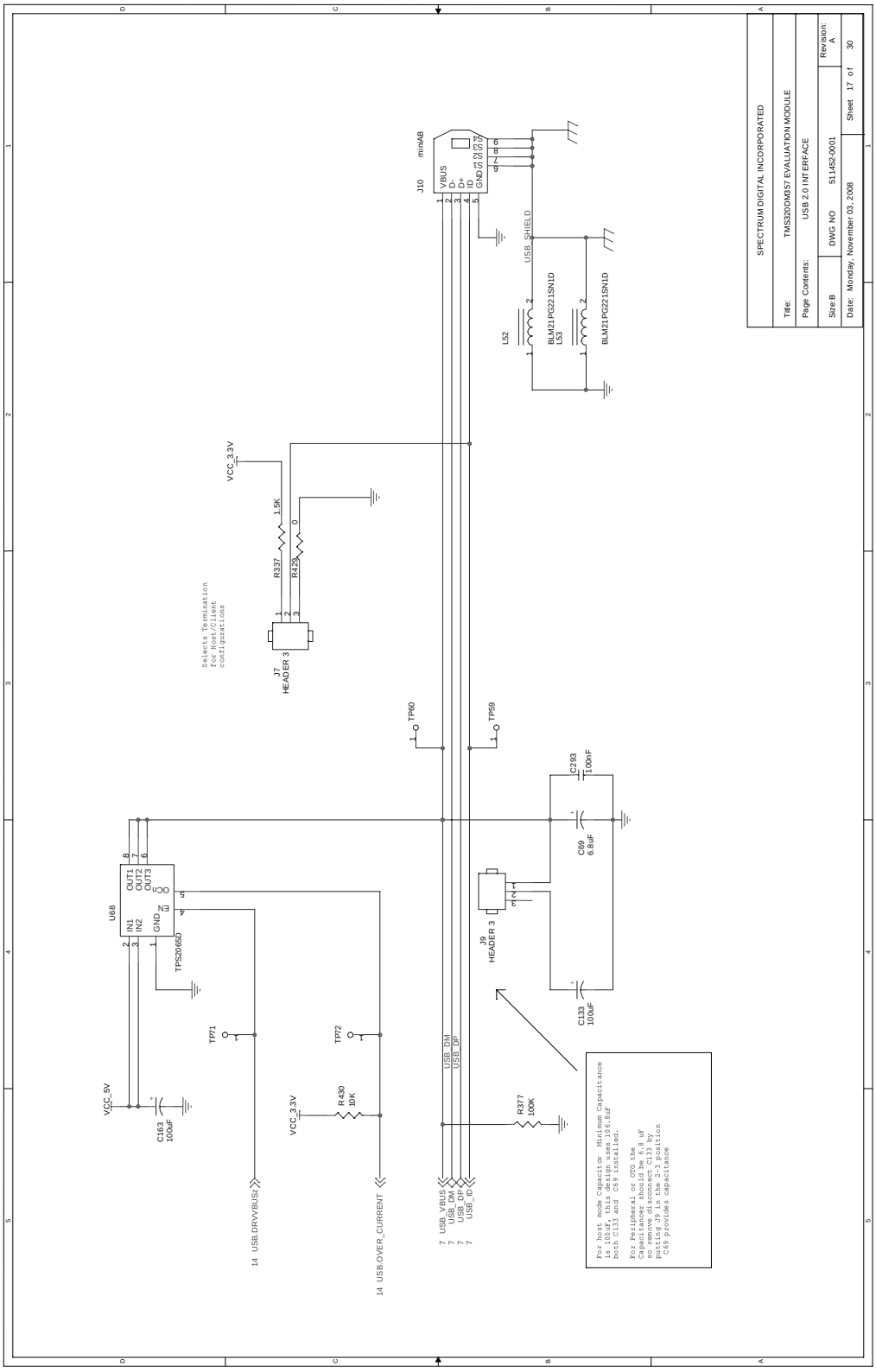

SPECTRUM DIGITAL INCORPORATED
Title: TMS320DM357 EVALUATION MODULE
Page Contents: SRAM/NAND FLASH
Size:B DWG NO 511452-0001 Revision: A
Date: Monday, November 03, 2008 Sheet 12 of 30
NAND FLASH (64MBytes)
K9K1G08 supports 128 MEGABITES
SAMSUNG K9K1208/Q/D/U/0C
U6
VCC_1.8V
R141 10K
R135 10K
R140 10K
R139 NO-POP
R113 NO-POP
C92 1uF
C93 1uF
R/B
RE
CE
CLE
ALE
WE
WP
LOCKPRE
VCC.1
VCC.2
VSS.1
VSS.2
VSS.3
NAND_BUSY
READ_OE
NAND_CE
CLE_EM_A2
ALE_EM_A1
WRITE_WE
EM_D7
EM_D6
EM_D5
EM_D4
EM_D3
EM_D2
EM_D1
EM_D0

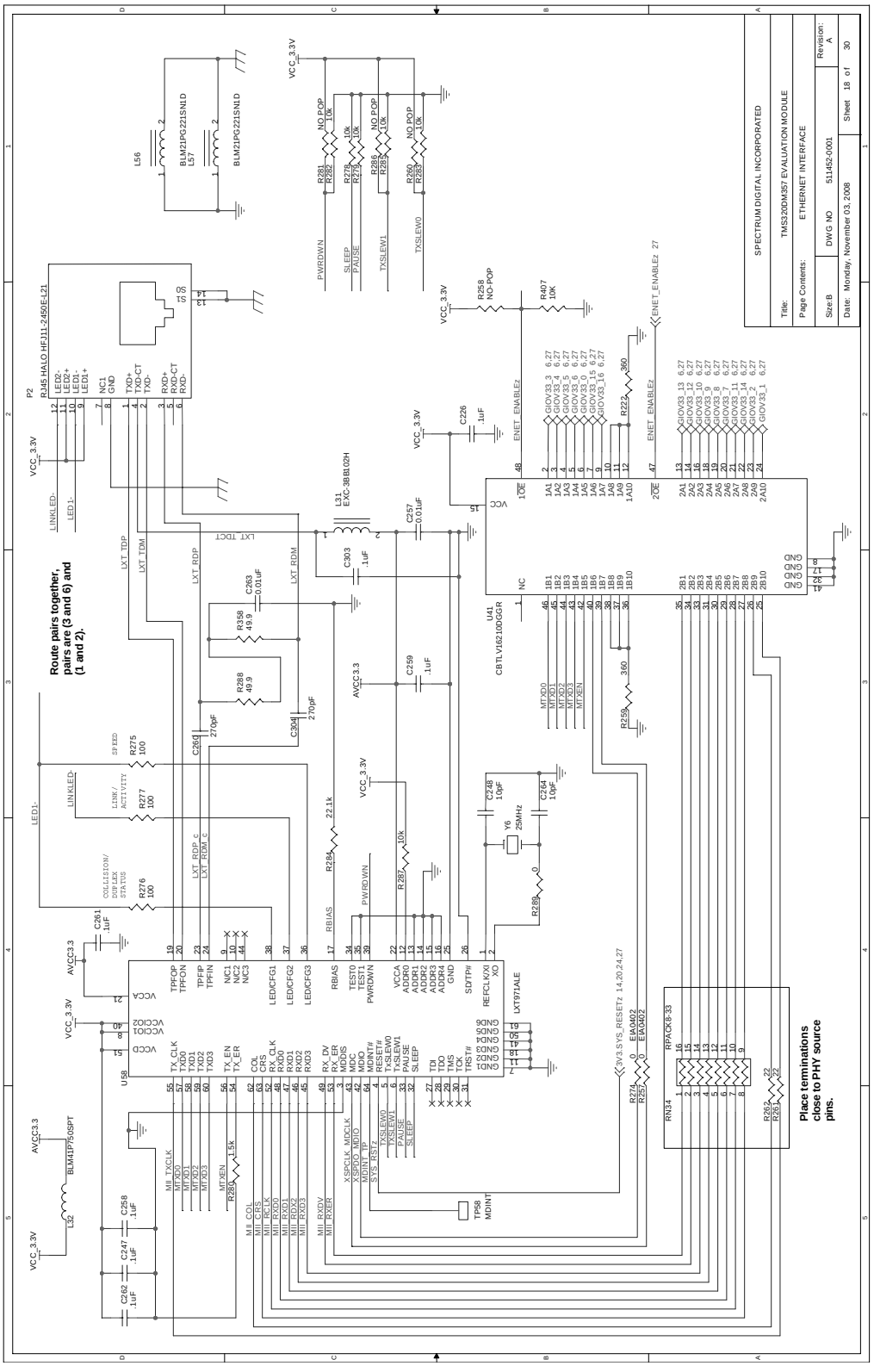

SPECTRUM DIGITAL INCORPORATED
Title: TMS320DM357 EVALUATION MODULE
Page Contents: EMIF LEVEL SHIFTER
Size:B DWG NO 5114452-0001 Revision: A
Date: Monday, November 03, 2008 Sheet 13 of 30
U67
MT29F16G08FAAWC:A
VCC_3.3V
R431 10K
R432 10K
R433 0
R434 0
R435 0
R436 0
R437 10K
C375 0.1uF
C376 10uF
C377 0.1uF
3V3_NAND_BUSY
3V3_READ_OE
3V3_NAND_CE0z
3V3_NAND_CE1z
3V3_CLE_EM_A2
3V3_ALE_EM_A1
3V3_WRITE_WE
3V3_EM_D7
3V3_EM_D6
3V3_EM_D5
3V3_EM_D4
3V3_EM_D3
3V3_EM_D2
3V3_EM_D1
3V3_EM_D0

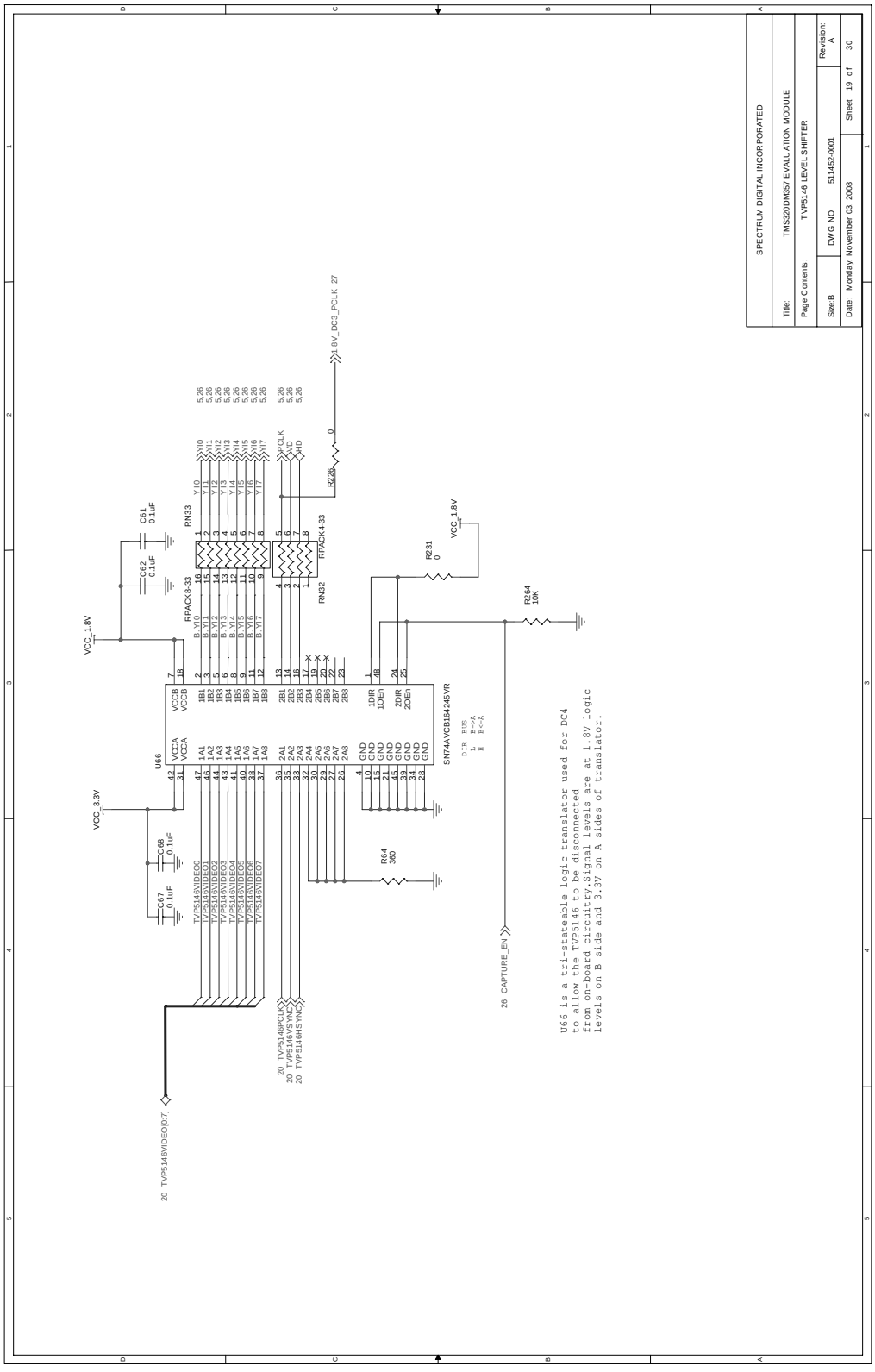

SPECTRUM DIGITAL INCORPORATED
Title: TMS320DM357 EVALUATION MODULE
Page Contents: CPLD DECODER/ LEVEL SHIFTER
Size: B
DWG NO 511452-0001
Revision: A
Date: Monday, November 03, 2008
Sheet 14 of 30
CPLD REVISION XXXXXX-0001A
EPM240GTC100
HEADER 6X2 2MM
SMT FEMALE HEADER 5X2
DIP_SWITCH_2
RPACK4-10K
NO-POP
BLM41P750SPT
LED
VCC_3.3V
VCC_1.8V
CPLD_TIMER_IN 5
MSP430_INT 24
3V3.DC_PCLK 5
USB.OVER_CURRENT 17
USB.DRVVBUSz 17
1V8.DC_PCLK
1.8V.SYS_RESETz
WAIT/BUSY
EM_RNW
WRITE_WE
READ_OE
TIMER_IN_DC3
GIO3
ISR_TCK
ISR_TDO
ISR_TMS
ISR_TDI
ISR_TDO

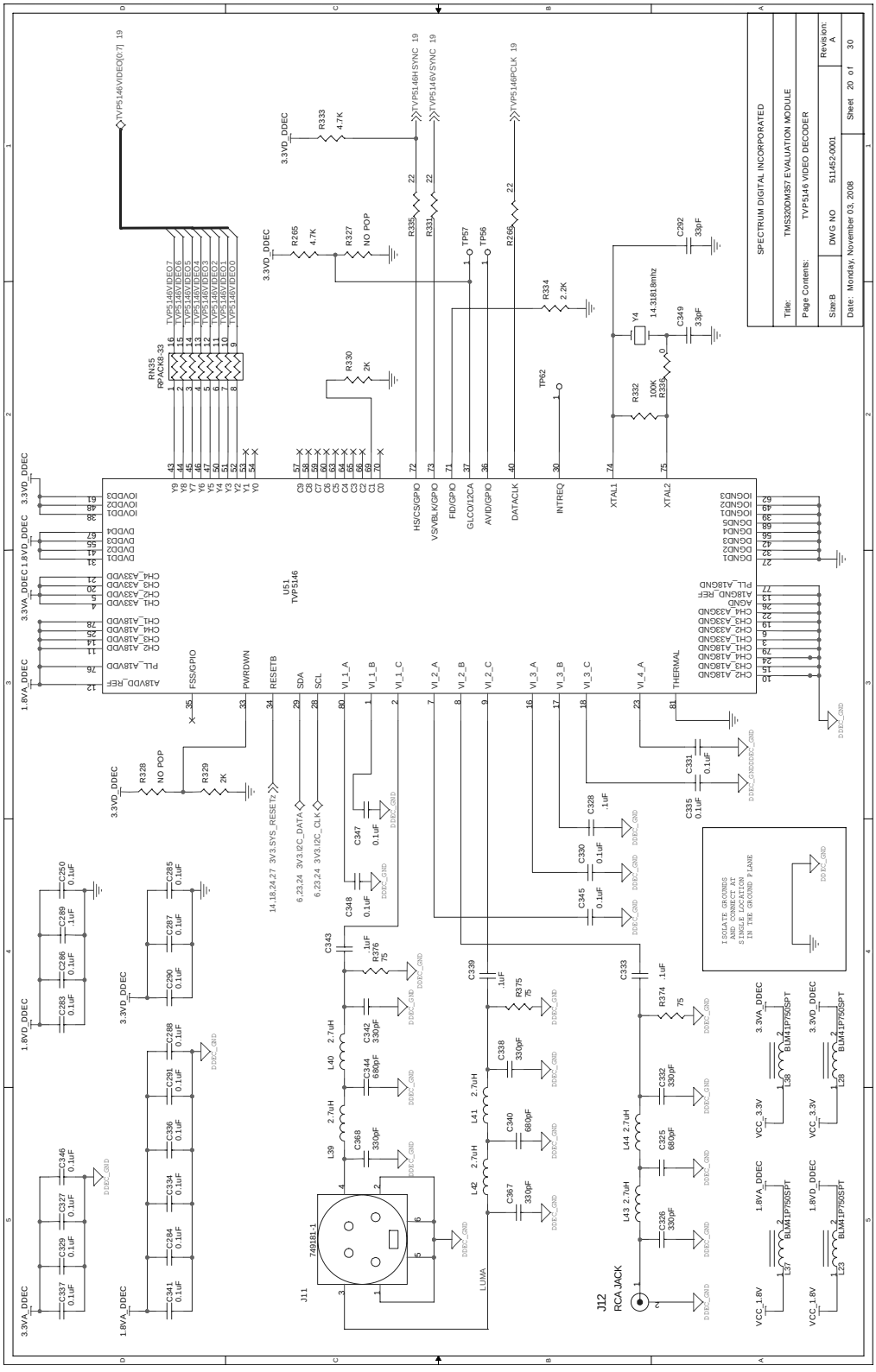

SPECTRUM DIGITAL INCORPORATED
Title: TMS320DM357 EVALUATION MODULE
Page Contents: SD/MMC CONNECTOR
Size: B
DWG NO 5114452-0001
Revision: A
Date: Monday, November 03, 2008
Sheet 15 of 30
SD/MMC.WP 24
SD/MMC.INS 24
VCC_3.3V
R73 51K
R108 51K
R99 0
J3
MMC/SD_CARD
CARD DETECT
DAT2
DAT3
CMD
VSS1
VDD
CLK
VSS2
DAT0
DAT1
C78 .1uF
C10 10uF
SD_DATA2
SD_DATA3
SD_CMD
SD_CLK
SD_DATA0
SD_DATA1
R117 51K
R126 51K
R120 51K
R122 51K
R124 51K
R123 51K
R118 NO-POP
R125 NO-POP
R119 NO-POP
7.27 SD_DATA2
7.27 SD_DATA3
7.27 SD_CMD
7.27 SD_CLK
7.27 SD_DATA0
7.27 SD_DATA1

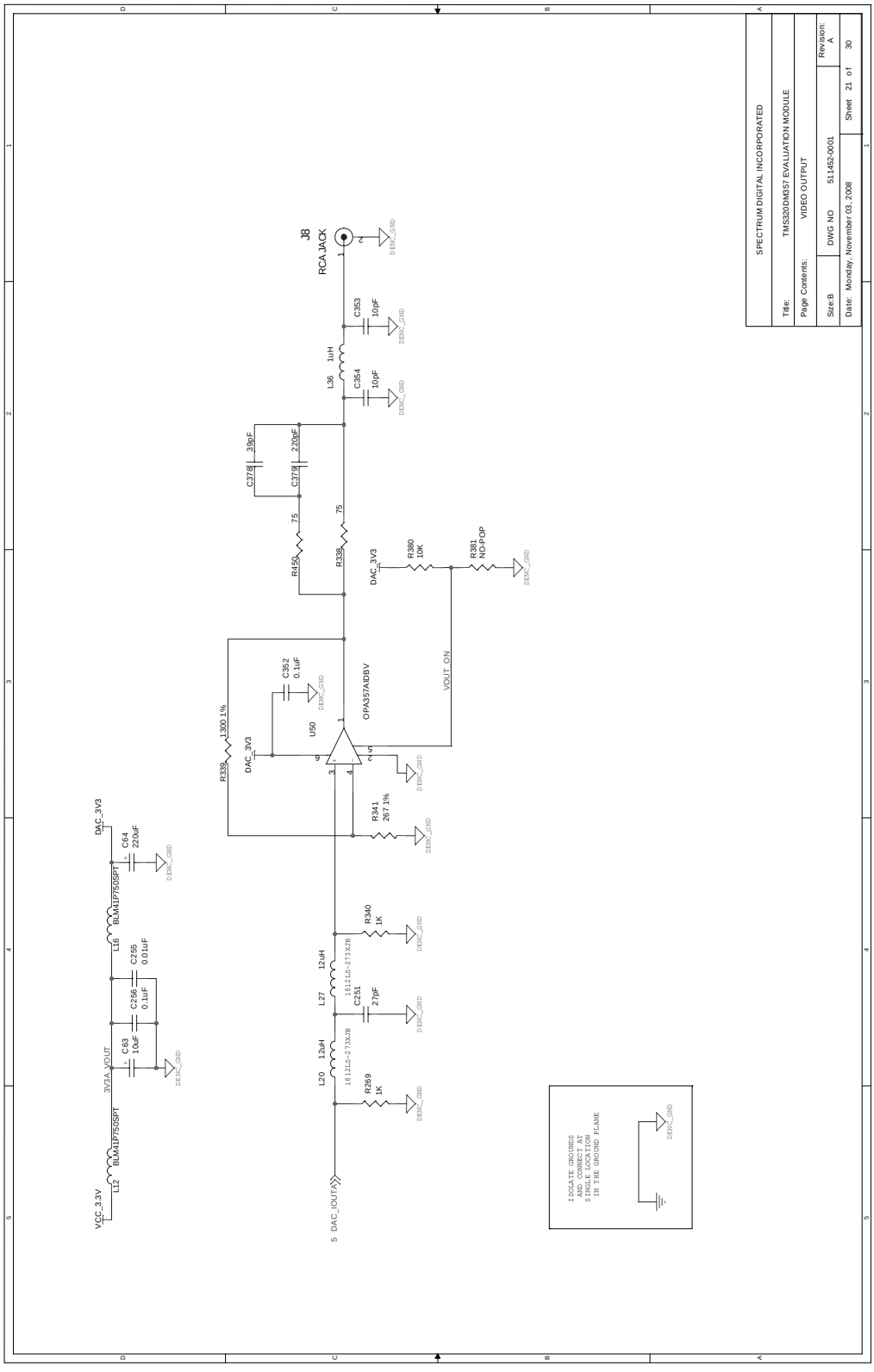

SPECTRUM DIGITAL INCORPORATED
Title: TMS320DM357 EVALUATION MODULE
Page Contents: RS232 INTERFACE
Size:B DWG NO 511452-0001 Revision: A
Date: Monday, November 03, 2008 Sheet 16 of 30
P6
DSUB9-Male
S_A_RXD
S_A_TXD
L54
BLM21PG221SN1D
L55
BLM21PG221SN1D
C297 10pF
C295 10pF
L46 1uH
L47 1uH
C300 10pF
C294 10pF
R354 10K
R355 10K
VCC_3.3V
C298 1uF
C296 1uF
U64
MAX221
DOUT
FORCEOFF
FORCEON
RIN
C2+
C2-
V-
GND
VCC
DIN
INVALID
ROUT
ENABLE
C1+
C1-
V+
C299 1uF
C77 47uF
C301 .1uF
C302 1uF
R356 0
R357 10
3V3.UART_TXD0
3V3.UART_RXD0
C246 .1uF
C244 .1uF
U42
U43
SN74AVC1T45
VCCA
VCCB
A1
B1
DIR
GND1
C245 .1uF
C243 .1uF
VCC_1.8V
UART_TXD0
UART_RXD0
6 UART_TXD0
6 UART_RXD0
DIR FUNCTION
L B-->A
H A-->B

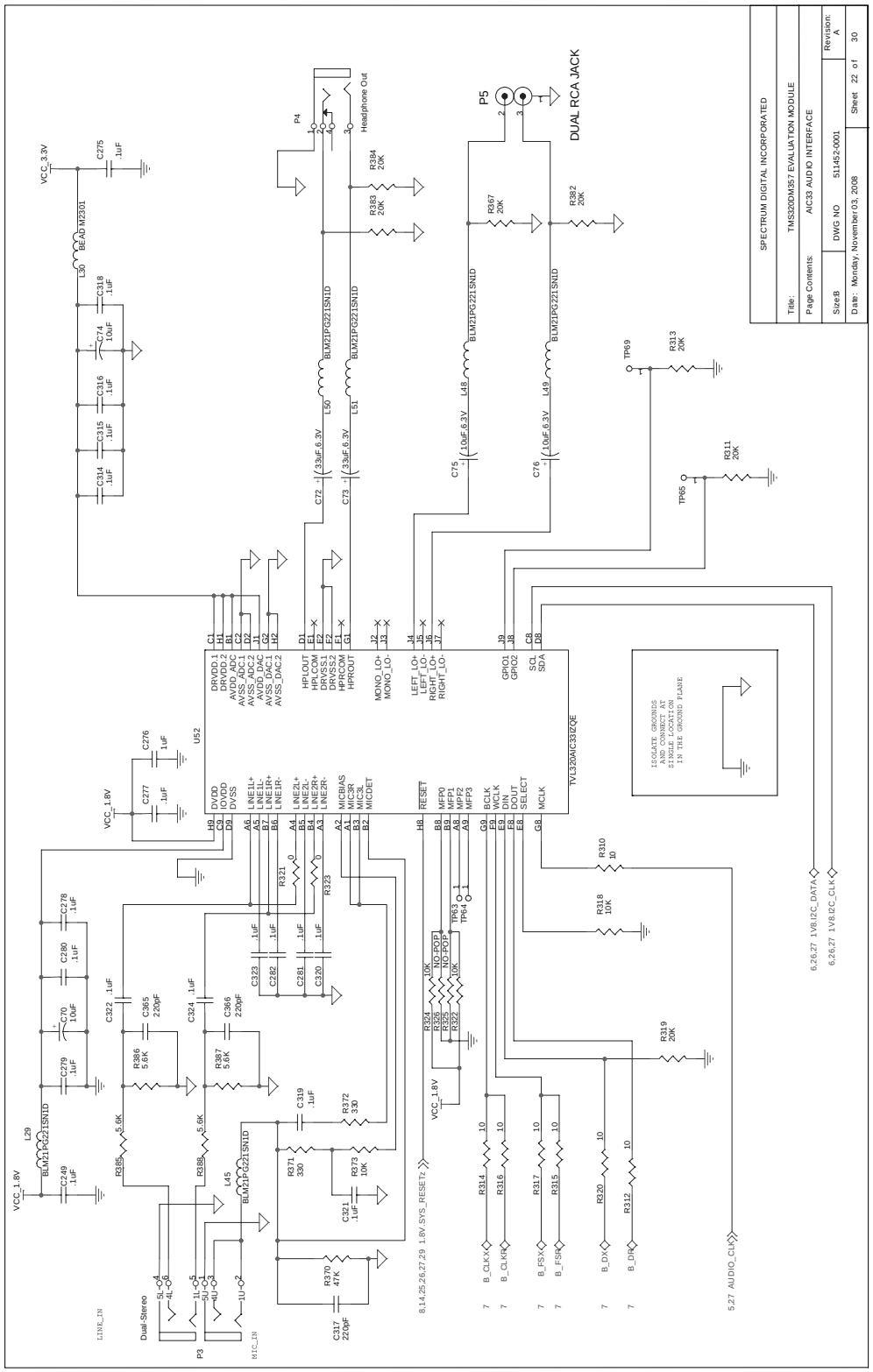

SPECTRUM DIGITAL INCORPORATED
Title: TMS320DM357 EVALUATION MODULE
Page Contents: USB 2.0 INTERFACE
Size:B
DWG NO 511452-0001
Revision: A
Date: Monday, November 03, 2008
Sheet 17 of 30
J10 miniAB
VBUS
D-
D+
ID
GND
USB_SHIELD
L52
BLM21PG221SN1D
L53
BLM21PG221SN1D
VCC_3.3V
R337 1.5K
R429 0
J7 HEADER 3
Selects Termination for Host/Client configurations
TP60
TP59
C293 100nF
C69 6.8uF
J9 HEADER 3
C133 100uF
U68
IN1
IN2
OUT1
OUT2
OUT3
OCn
EN
GND
TPS2065D
TP71
TP72
VCC_5V
C163 100uF
VCC_3.3V
R430 10K
R377 100K
USB_DM
USB_DP
14 USB.DRVVBUSz
14 USB.OVER_CURRENT
7 USB_VBUS
7 USB_DM
7 USB_DP
7 USB_ID
For host mode Capacitor Minimum Capacitance is 100uF, this design uses 106.8uF both C133 and C69 installed.
For Peripheral or OTG the Capacitancer should be 6.8 uF so remove disconnect C133 by putting J9 in the 2-3 position C69 provides capacitance

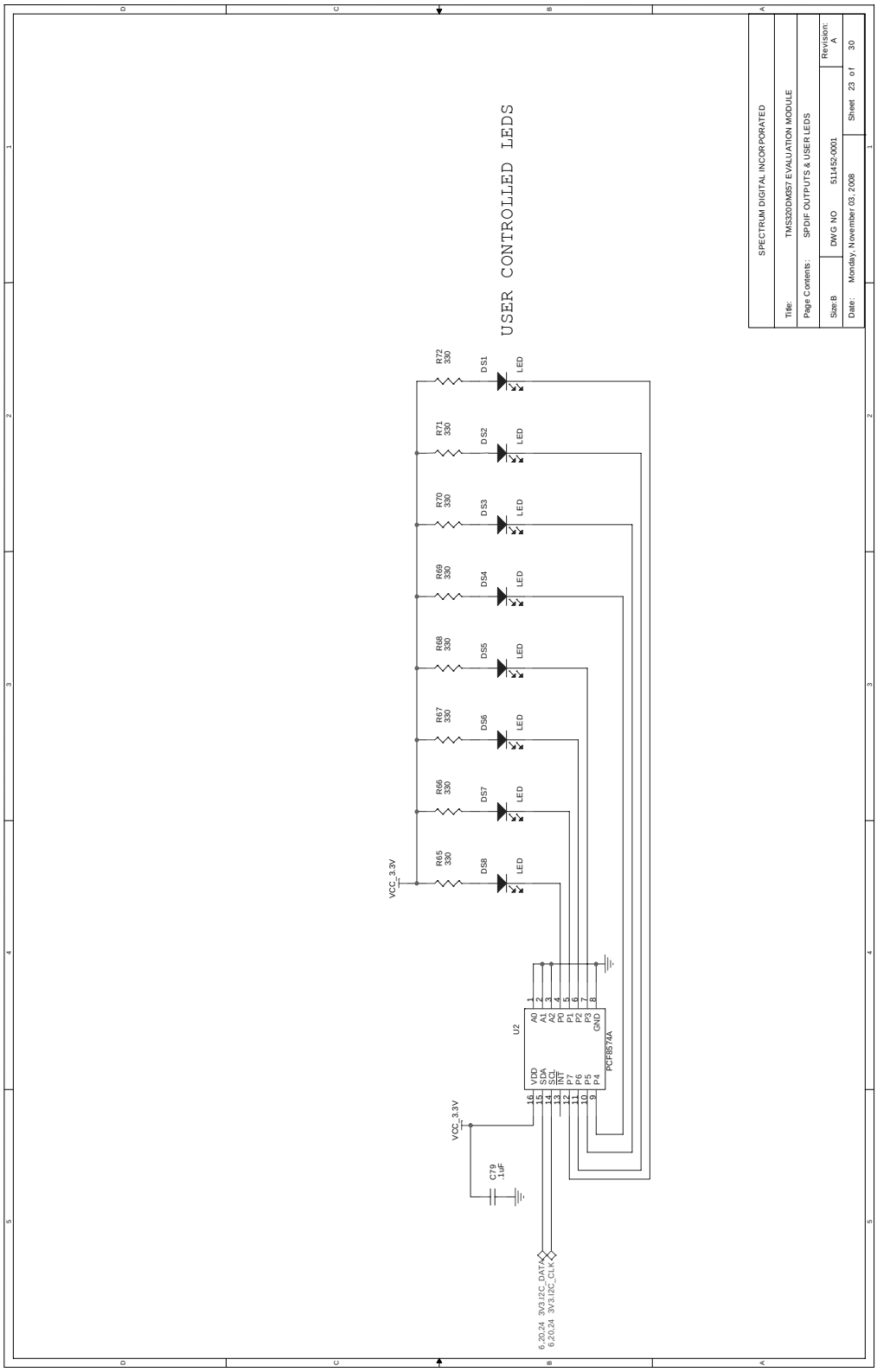

Route pairs together, pairs are (3 and 6) and (1 and 2).
Place terminations close to PHY source pins.
SPECTRUM DIGITAL INCORPORATED
Title: TMS320DM357 EVALUATION MODULE
Page Contents: ETHERNET INTERFACE
Size:B DWG NO 511452-0001 Revision: A
Date: Monday, November 03, 2008 Sheet 18 of 30
U58 LXT971ALE
U41 CBTLV16210DGGR
P2 RJ45 HALO HFJ11-2450E-L21
Y6 25MHz
RPACK8-33
L56 BLM21PG221SN1D
L57 BLM21PG221SN1D
L52 BLM41P750SPT
L31 EXC-38BL02H

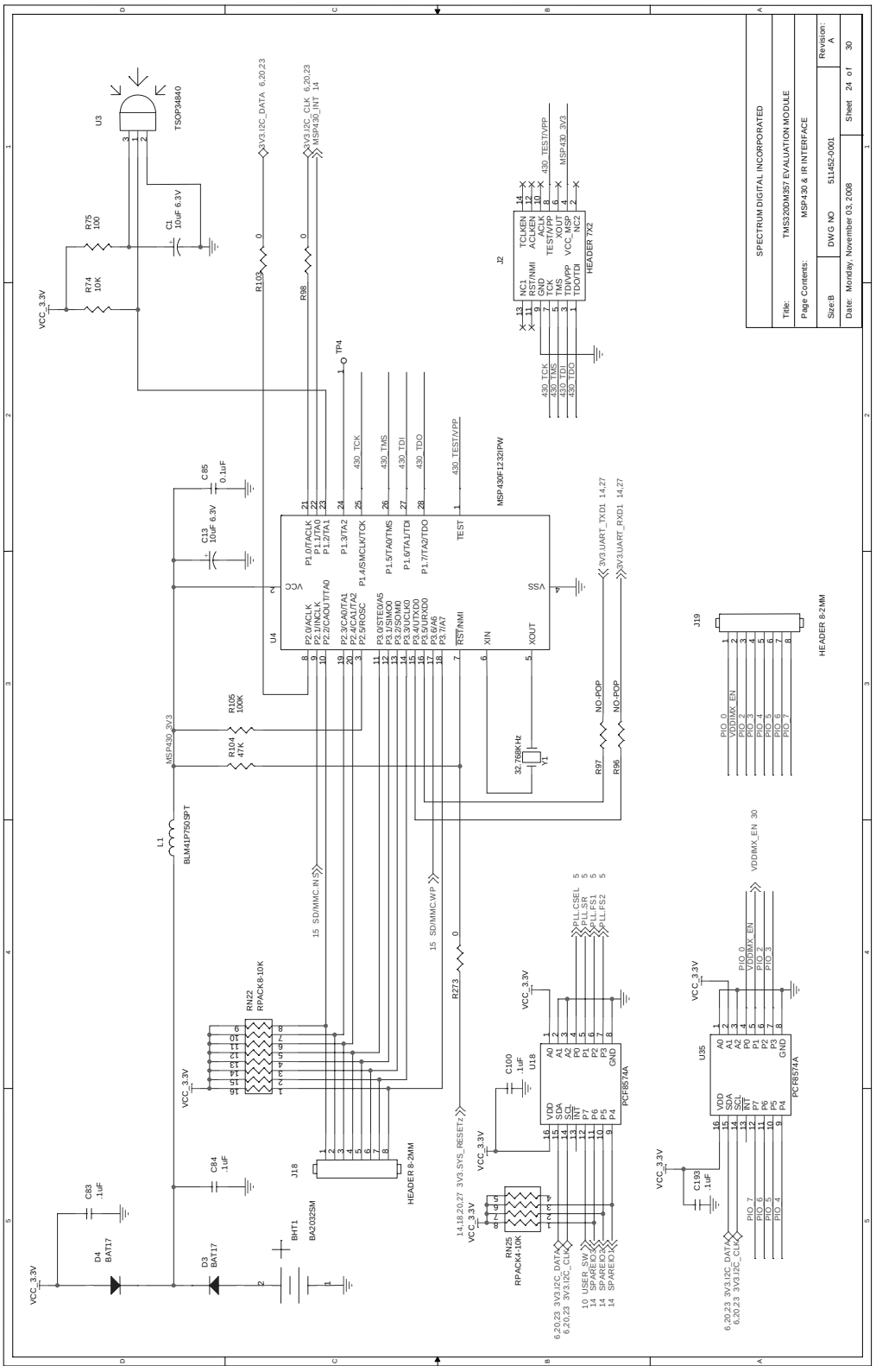

SPECTRUM DIGITAL INCORPORATED
Title: TMS320DM357 EVALUATION MODULE
Page Contents: TVP5146 LEVEL SHIFTER
Size:B DWG NO 511452-0001 Revision: A
Date: Monday, November 03, 2008 Sheet 19 of 30
U66
SN74AVCB164245VR
RPACK8-33
RPACK4-33
RN33
RN32
VCC_3.3V
VCC_1.8V
1.8V_DC3_PCLK 27
R226 0
R231 0
R64 360
R264 10K
C61 0.1uF
C62 0.1uF
C67 0.1uF
C68 0.1uF
20 TVP5146VIDEO[0:7]
20 TVP5146PCLK
20 TVP5146VSYNC
20 TVP5146HSYNC
26 CAPTURE_EN
U66 is a tri-stateable logic translator used for DC4
to allow the TVP5146 to be disconnected
from on-board circuitry. Signal levels are at 1.8V logic
levels on B side and 3.3V on A sides of translator.

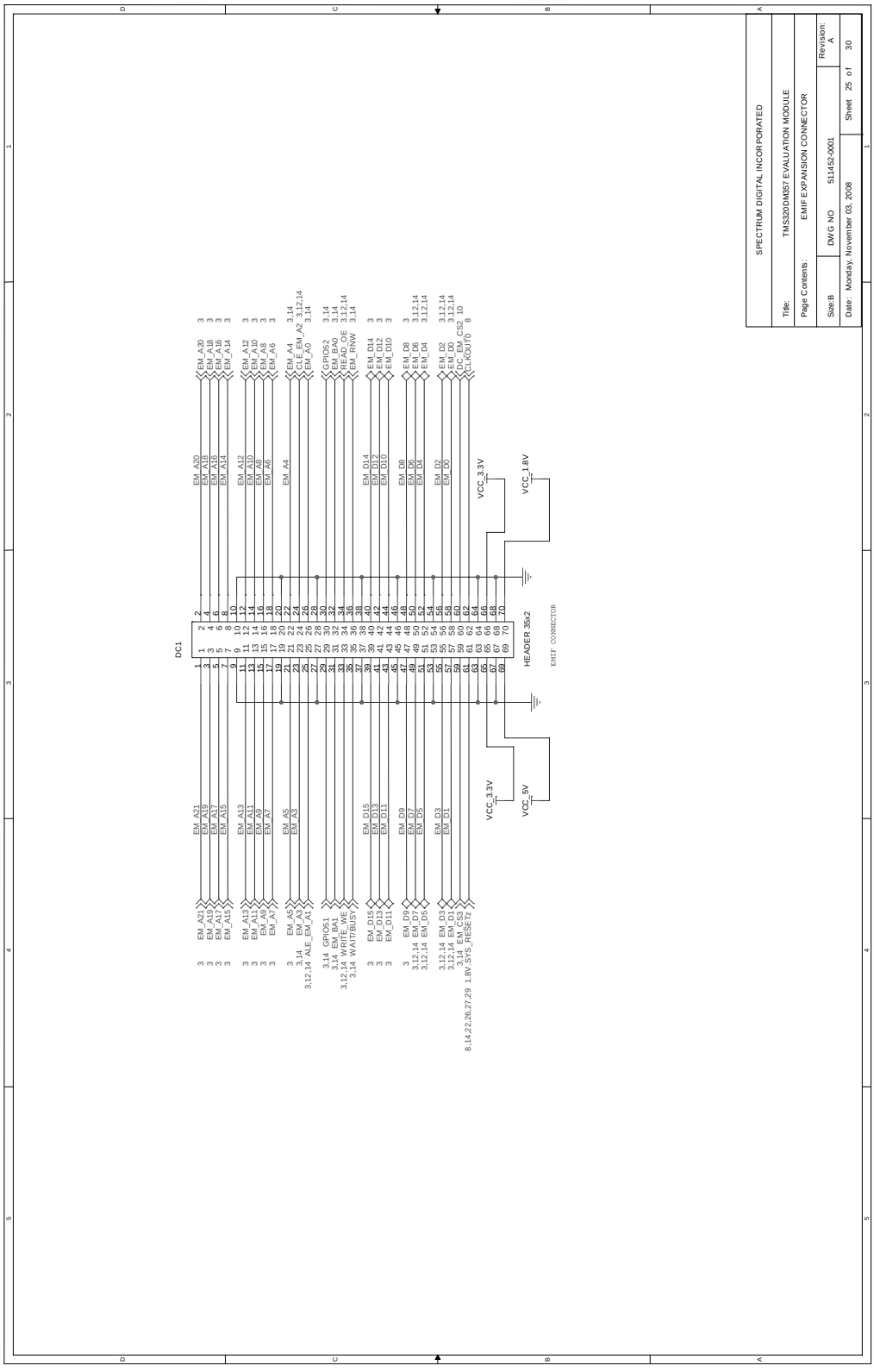

SPECTRUM DIGITAL INCORPORATED
Title: TMS320DM357 EVALUATION MODULE
Page Contents: TVP5146 VIDEO DECODER
Size:B DWG NO. 511452-0001 Revision: A
Date: Monday, November 03, 2008 Sheet 20 of 30
U51 TVP5146
TVP5146VIDEO[0:7] 19
TVP5146HSYNC 19
TVP5146VSYNC 19
TVP5146PCLK 19
RN35 RPACK8-33
R265 4.7K
R327 NO POP
R330 2K
R333 4.7K
R335 22
R331 22
R265 22
R334 2.2K
R332 10K
R336 0
Y4 14.31818mhz
C292 33pF
C349 33pF
TP57
TP56
TP62
R328 NO POP
R329 2K
14,18,24,27 3V3.SYS_RESETz
6,23,24 3V3.I2C_DATA
6,23,24 3V3.I2C_CLK
ISOLATE GROUNDS AND CONNECT AT SINGLE LOCATION TO THE GROUND PLANE
J11 749181-1
J12 RCA JACK
LUMA
3.3VD_DDEC
1.8VD_DDEC
3.3VA_DDEC
1.8VA_DDEC
VCC_3.3V
VCC_1.8V
1.8VA_DDEC
1.8VD_DDEC
3.3VA_DDEC
3.3VD_DDEC
BLM41P750SPT

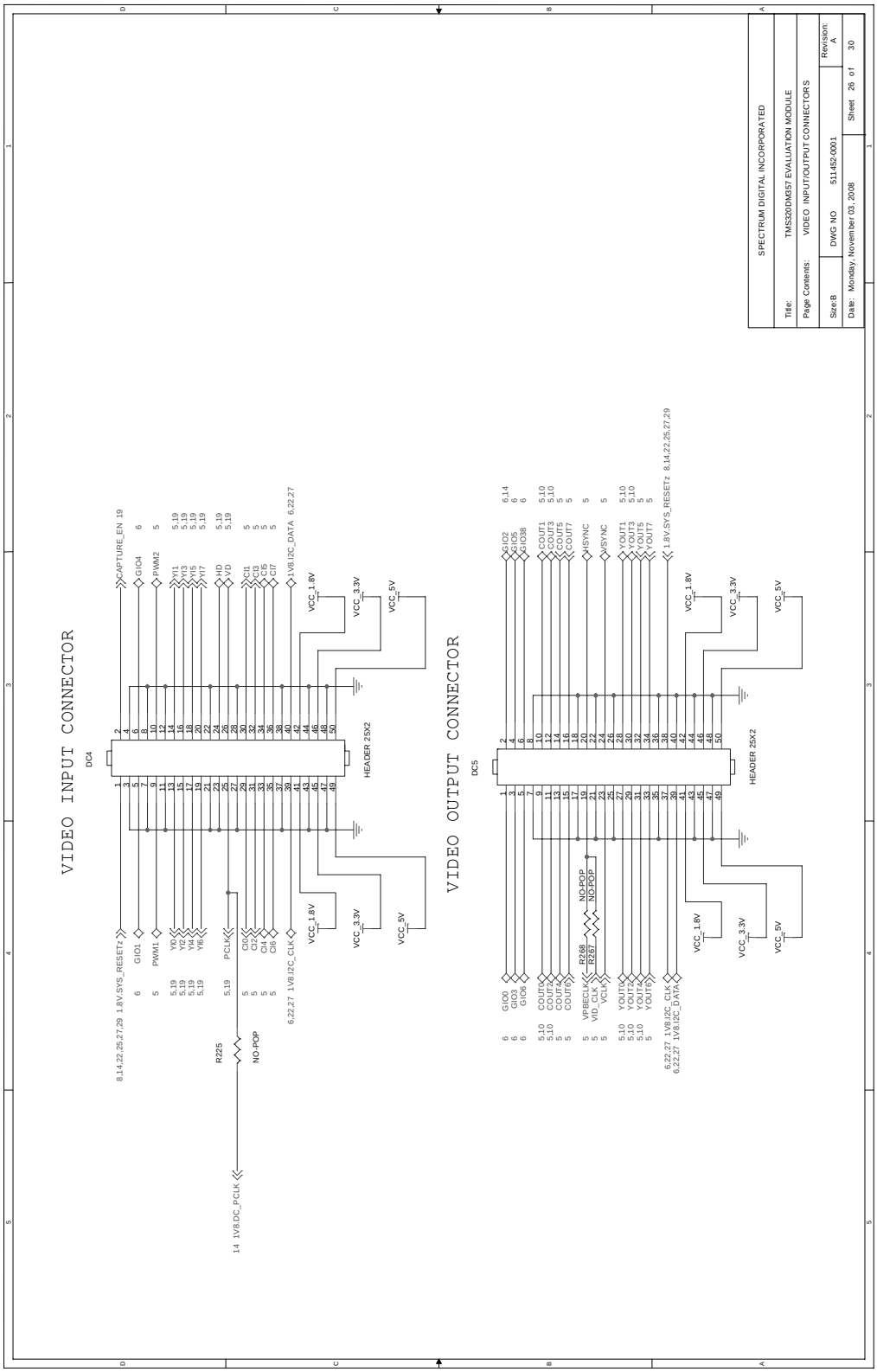

SPECTRUM DIGITAL INCORPORATED
Title: TMS320DM357 EVALUATION MODULE
Page Contents: VIDEO OUTPUT
Size: B
DWG NO 511452-0001
Revision: A
Date: Monday, November 03, 2008
Sheet 21 of 30
J8
RCA JACK
C353 10pF
C354 10pF
L36 1uH
C378 39pF
C379 220pF
R450 75
R398 75
R390 10K
R391 NO-POP
DAC_3V3
VOUT_ON
OPA357AIDBV
U50
C352 0.1uF
R339 1300 1%
R341 267 1%
R340 1K
L27 12uH
C251 270pF
L20 12uH
R269 1K
5 DAC_IOUT
VCC_3.3V
L12 BLM41PY500SPT
3V3A_VOUT
L16 BLM41PY500SPT
C64 220uF
C255 0.01uF
C256 0.1uF
C63 10uF
ISOLATE GROUNDS AND CONNECT AT A SINGLE LOCATION IN THE GROUND PLANE
DENC_GND


SPECTRUM DIGITAL INCORPORATED
Title: TMS320DM357 EVALUATION MODULE
Page Contents: AIC33 AUDIO INTERFACE
Size:B
DWG NO 511452-0001
Revision: A
Date: Monday, November 03, 2008
Sheet 22 of 30
DUAL RCA JACK
Headphone Out
Dual Stereo
TVL320AIC3312CQE
BLM21PG221SN1D
ISOLATE GROUNDS AND CONNECT AT SINGLE POINT TO THE GROUND PLANE


USER CONTROLLED LEDS
SPECTRUM DIGITAL INCORPORATED
Title: TMS320DM357 EVALUATION MODULE
Page Contents: SPDIF OUTPUTS & USER LEDS
Size: B
DWG NO 511452-0001
Revision: A
Date: Monday, November 03, 2008
Sheet 23 of 30
R72 330
R71 330
R70 330
R69 330
R68 330
R67 330
R66 330
R65 330
DS1 LED
DS2 LED
DS3 LED
DS4 LED
DS5 LED
DS6 LED
DS7 LED
DS8 LED
VCC_3.3V
U2
PCF8574A
A0 A1 A2 P0 P1 P2 P3 GND
VDD SDA SCL INT P7 P6 P5 P4
C79 .1uF
6,20,24 3V3.I2C_DATA
6,20,24 3V3.I2C_CLK


SPECTRUM DIGITAL INCORPORATED
Title: TMS320DM357 EVALUATION MODULE
Page Contents: MSP430 & IR INTERFACE
Size:B DWG NO 511452-0001 Revision: A
Date: Monday, November 03, 2008 Sheet 24 of 30
U3
TSOP34840
R75 100
R74 10K
C1 10uF 6.3V
R103 0
R98 0
3V3.I2C_DATA 6,20,23
3V3.I2C_CLK 6,20,23
MSP430_INT 14
VCC_3.3V
J2
HEADER 7X2
430_TCK
430_TMS
430_TDI
430_TDO
430_TEST/VPP
MSP430_3V3
TP4
C85 0.1uF
C13 10uF 6.3V
U4
MSP430F1232IPW
P1.0/TACLK
P1.1/TA0
P1.2/TA1
P1.3/TA2
P1.4/SMCLK/TCK
P1.5/TA0/TMS
P1.6/TA1/TDI
P1.7/TA2/TDO
TEST
RST/NMI
XIN
XOUT
VCC
VSS
P2.0/ACLK
P2.1/INCLK
P2.2/CAOUT/TA0
P2.3/CA0/TA1
P2.4/CA1/TA2
P2.5/ROSC
P3.0/STE0/A5
P3.1/SIMO0
P3.2/SOMI0
P3.3/UCLK0
P3.4/UTXD0
P3.5/URXD0
P3.6/A6
P3.7/A7
R105 100K
R104 47K
MSP430_3V3
L1
BLM41P750SPT
Y1
32.768KHz
R97 NO-POP
R96 NO-POP
3V3.UART_TXD1 14,27
3V3.UART_RXD1 14,27
J19
HEADER 8-2MM
PIO_0
VDDIMX_EN
PIO_2
PIO_3
PIO_4
PIO_5
PIO_6
PIO_7
15 SD/MMC.IN
15 SD/MMC.WP
R273 0
RN22 RPACK8-10K
J18
HEADER 8-2MM
C84 .1uF
C83 .1uF
D4 BAT17
D3 BAT17
BHT1
BA2032SM
C100 1uF
U18
PCF8574A
P1.LL.CSEL 5
P1.LL.SR 5
P1.LL.FS1 5
P1.LL.FS2 5
VCC_3.3V
1,4,18,20,27 3V3.SYS_RESET
RN25 RPACK4-10K
6,20,23 3V3.I2C_DATA
6,20,23 3V3.I2C_CLK
10 USER_SW
14 SPARE(IO)
14 SPARE(IO)
14 SPARE(IO)
U35
PCF8574A
C193 .1uF
VDDIMX_EN 30
PIO_0
PIO_2
PIO_3
PIO_4
PIO_5
PIO_6
PIO_7
6,20,23 3V3.I2C_DATA
6,20,23 3V3.I2C_CLK


SPECTRUM DIGITAL INCORPORATED
Title: TMS320DM357 EVALUATION MODULE
Page Contents: EMIF EXPANSION CONNECTOR
Size:B
DWG NO 511452-0001
Revision: A
Date: Monday, November 03, 2008
Sheet 25 of 30
DC1
HEADER 35x2
EMIF CONNECTOR
VCC_3.3V
VCC_1.8V
VCC_5V
EM_A20
EM_A18
EM_A16
EM_A14
EM_A12
EM_A10
EM_A8
EM_A6
EM_A4
EM_A2
EM_A0
GPIO52
EM_WE
RE_AD_OE
EM_RNW
EM_D14
EM_D12
EM_D10
EM_D8
EM_D6
EM_D4
EM_D2
EM_D0
DC_EM_CS2
CLKOUT0
EM_A21
EM_A19
EM_A17
EM_A15
EM_A13
EM_A11
EM_A9
EM_A7
EM_A5
EM_A3
EM_A1
ALE_EM_A1
GPIO51
EM_WAIT
WRITE_WE
WAIT/BUSY
EM_D15
EM_D13
EM_D11
EM_D9
EM_D7
EM_D5
EM_D3
EM_D1
EM_CS3
1.8V_SYS_RESETz


VIDEO INPUT CONNECTOR
VIDEO OUTPUT CONNECTOR
DC4
DC5
HEADER 25X2
R225
NO-POP
R268
R267
VCC_1.8V
VCC_3.3V
VCC_5V
SPECTRUM DIGITAL INCORPORATED
Title: TMS320DM357 EVALUATION MODULE
Page Contents: VIDEO INPUT/OUTPUT CONNECTORS
Size:B
DWG NO 511452-0001
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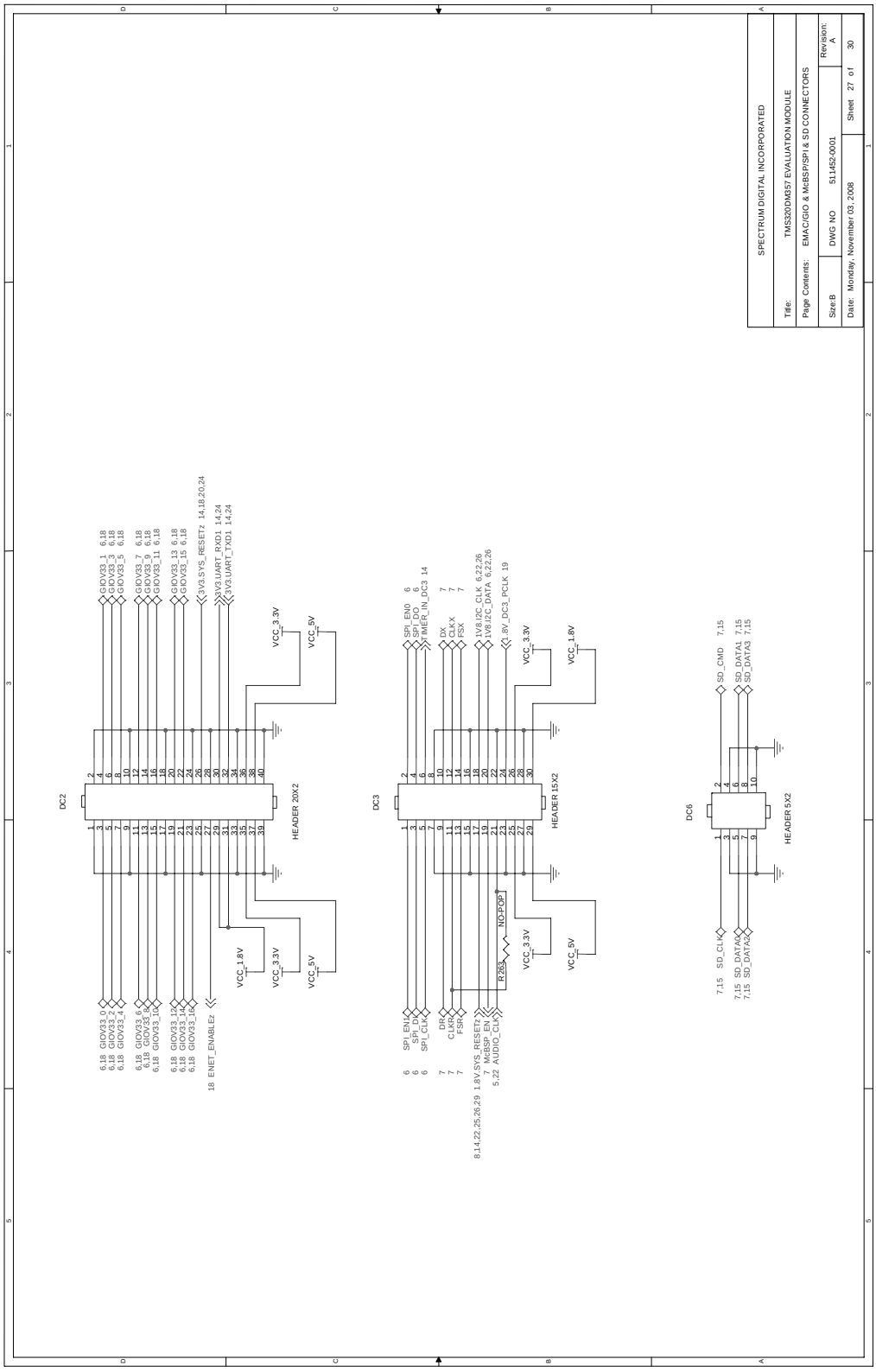
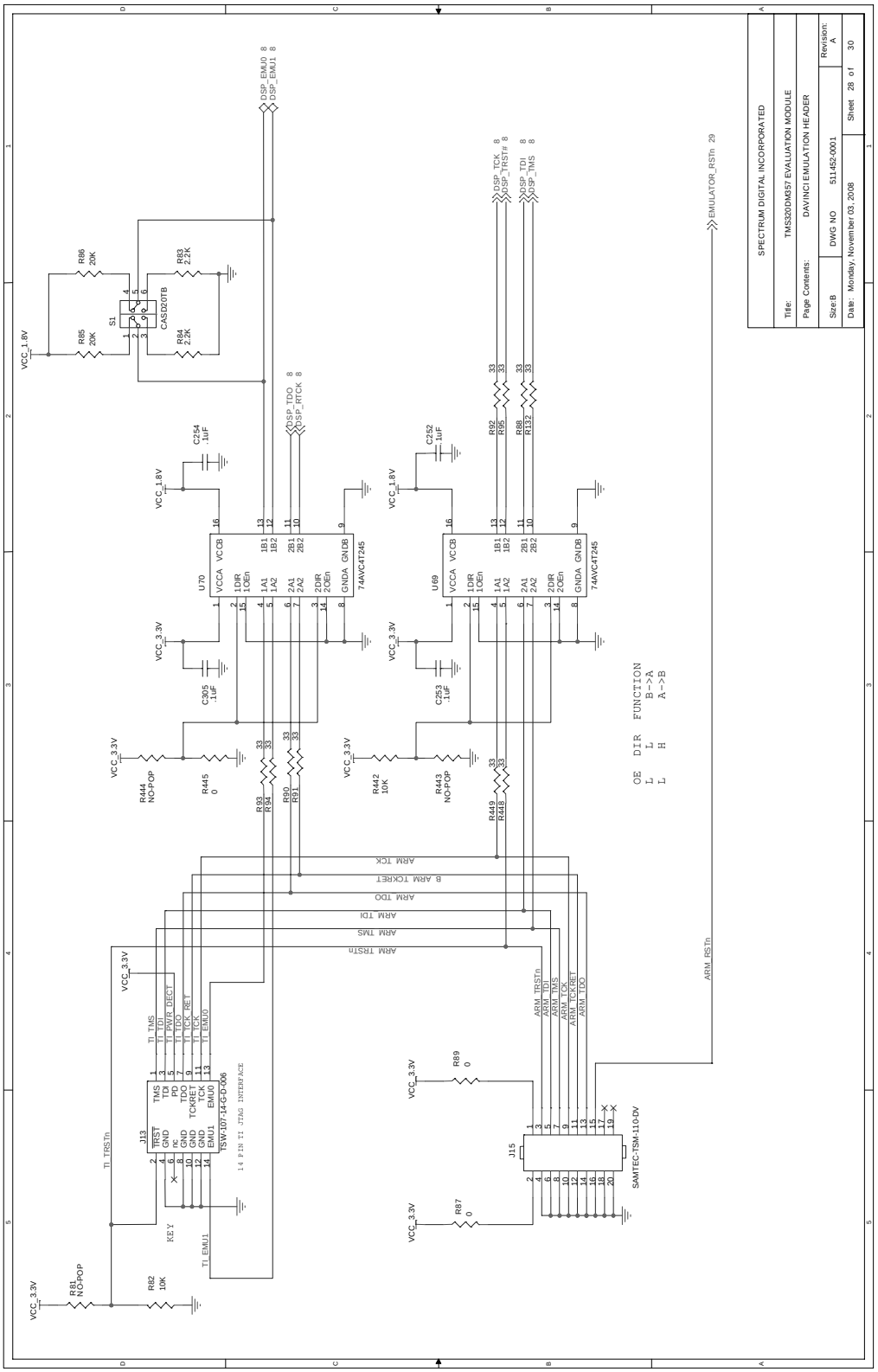
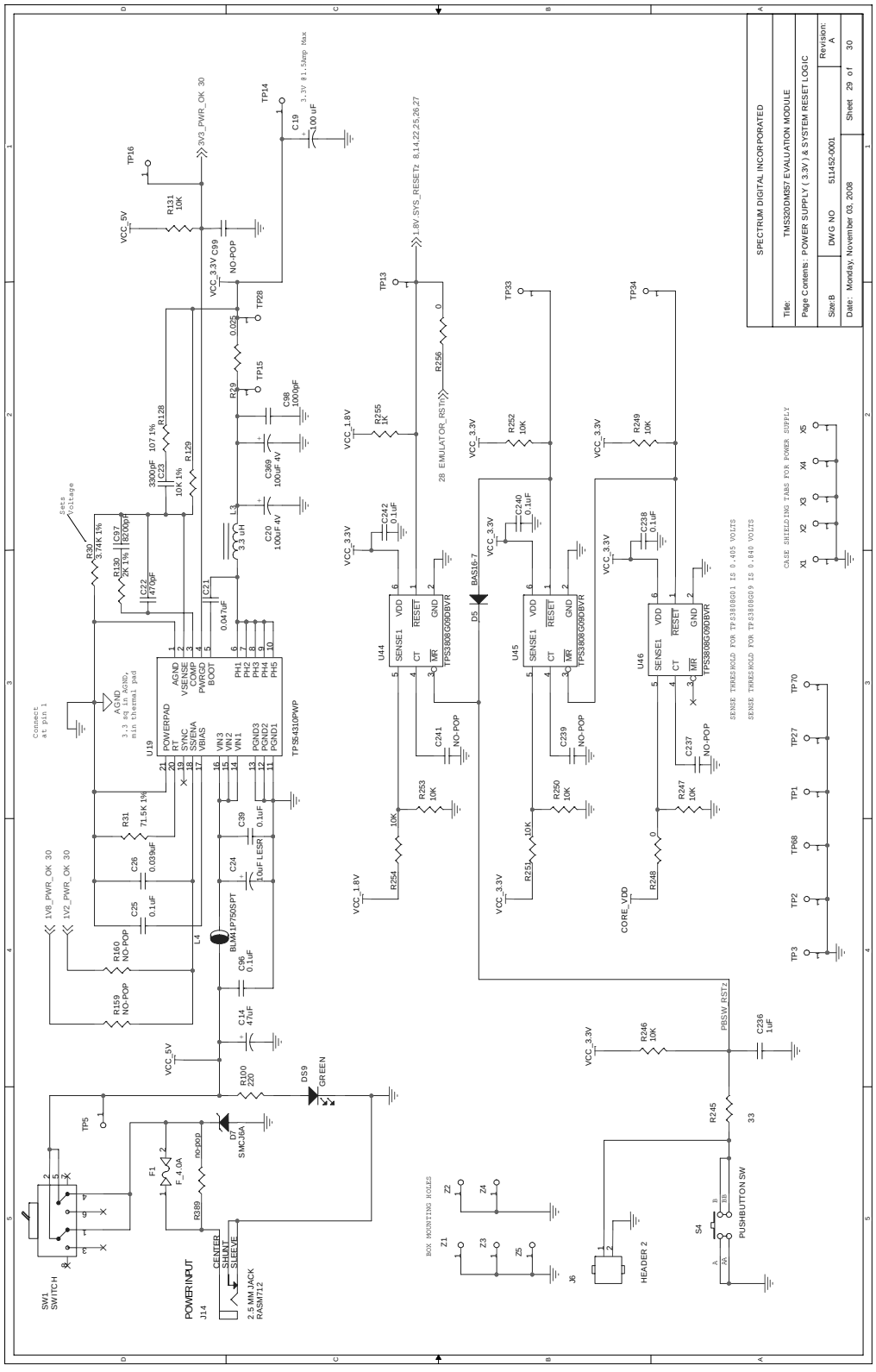
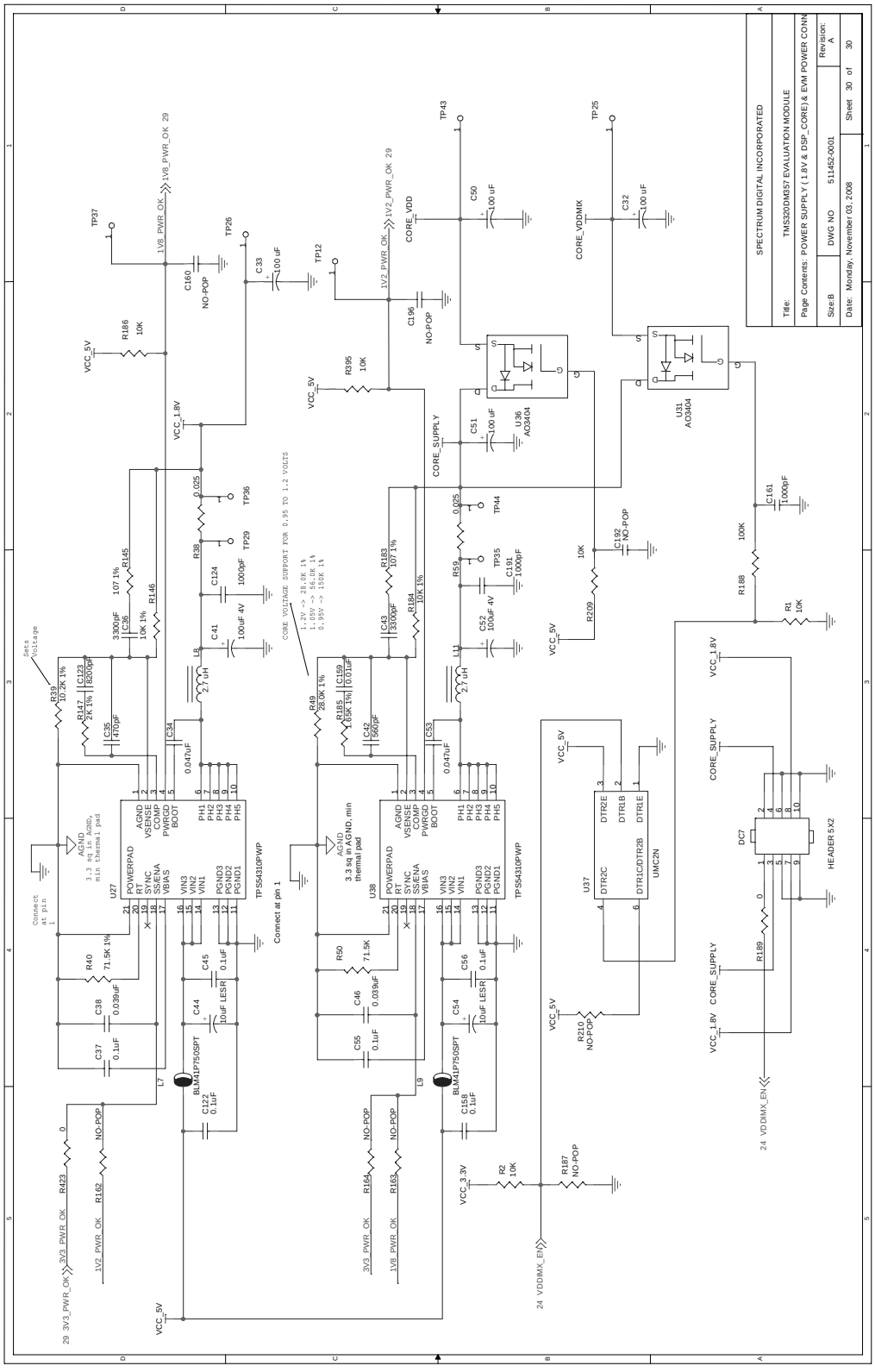
Sheet 26 of 30


SPECTRUM DIGITAL INCORPORATED
Title: TMS320DM357 EVALUATION MODULE
Page Contents: EMAC/GIO & McBSP/SPI & SD CONNECTORS
Size:B
DWG NO 511452-0001
Revision: A
Date: Monday, November 03, 2008
Sheet 27 of 30
DC2
HEADER 20X2
DC3
HEADER 15X2
DC6
HEADER 5X2
VCC_3.3V
VCC_5V
VCC_1.8V
R265
NO-POP


SPECTRUM DIGITAL INCORPORATED
Title: TMS320DM357 EVALUATION MODULE
Page Contents: DAVINCI EMULATION HEADER
Size:B
DWG NO 511452-0001
Revision: A
Date: Monday, November 03, 2008
Sheet 28 of 30
EMULATOR_RSTn 29
DSP_EMU0 8
DSP_EMU1 8
DSP_TDO 8
DSP_RTCK 8
DSP_TCK 8
DSP_TRST# 8
DSP_TDI 8
DSP_TMS 8
U70
U69
74AVC4T245
VCCA VCCB
GNDA GNDB
1DIR 1OEn
2DIR 2OEn
1A1 1A2 2A1 2A2
1B1 1B2 2B1 2B2
OE DIR FUNCTION
L L B->A
L H A->B
S1
CAS-D20TB
J13
TSW-107-14-G-D-006
14 PIN TI JTAG INTERFACE
J15
SAMTEC-TSM-110-DV
KEY
TI_TMS
TI_TDI
TI_RTCK_DETECT
TI_TDO
TI_TCK_RET
TI_TCK
TI_EMU0
TI_EMU1
TI_TRSTn
ARM_TRSTn
ARM_TMS
ARM_TDI
ARM_TDO
ARM_TCKRET
ARM_TCK
ARM_RSTn
VCC_1.8V
VCC_3.3V


SPECTRUM DIGITAL INCORPORATED
Title: TMS320DM357 EVALUATION MODULE
Page Contents: POWER SUPPLY (3.3V) & SYSTEM RESET LOGIC
Size:B
DWG NO 511452-0001
Revision: A
Date: Monday, November 03, 2008
Sheet 29 of 30
TPS54310PWP
TPS3808G09DBVR
POWERINPUT
J14
2.5 MM JACK
RASM712
SW1
SWITCH
HEADER 2
PUSHBUTTON SW
BOX MOUNTING HOLES
CASE SHIELDING TABS FOR POWER SUPPLY
SENSE THRESHOLD FOR TPS3808G01 IS 0.405 VOLTS
SENSE THRESHOLD FOR TPS3808G09 IS 0.840 VOLTS
28 EMULATOR_RSTn
1.8V_SYS_RESETz 8,14,22,25,26,27
3V3_PWR_OK 30
1V8_PWR_OK 30
1V2_PWR_OK 30
CORE_VDD
PBSW_RSTz
VCC_5V
VCC_3.3V
VCC_1.8V
Sets Voltage
Connect at pin 1
AGND 3.3 sq in AGND, min thermal pad


SPECTRUM DIGITAL INCORPORATED
Title: TMS320DM357 EVALUATION MODULE
Page Contents: POWER SUPPLY (1.8V & DSP_CORE) & EVM POWER CONN
Size:B DWG NO 511452-0001 Revision: A
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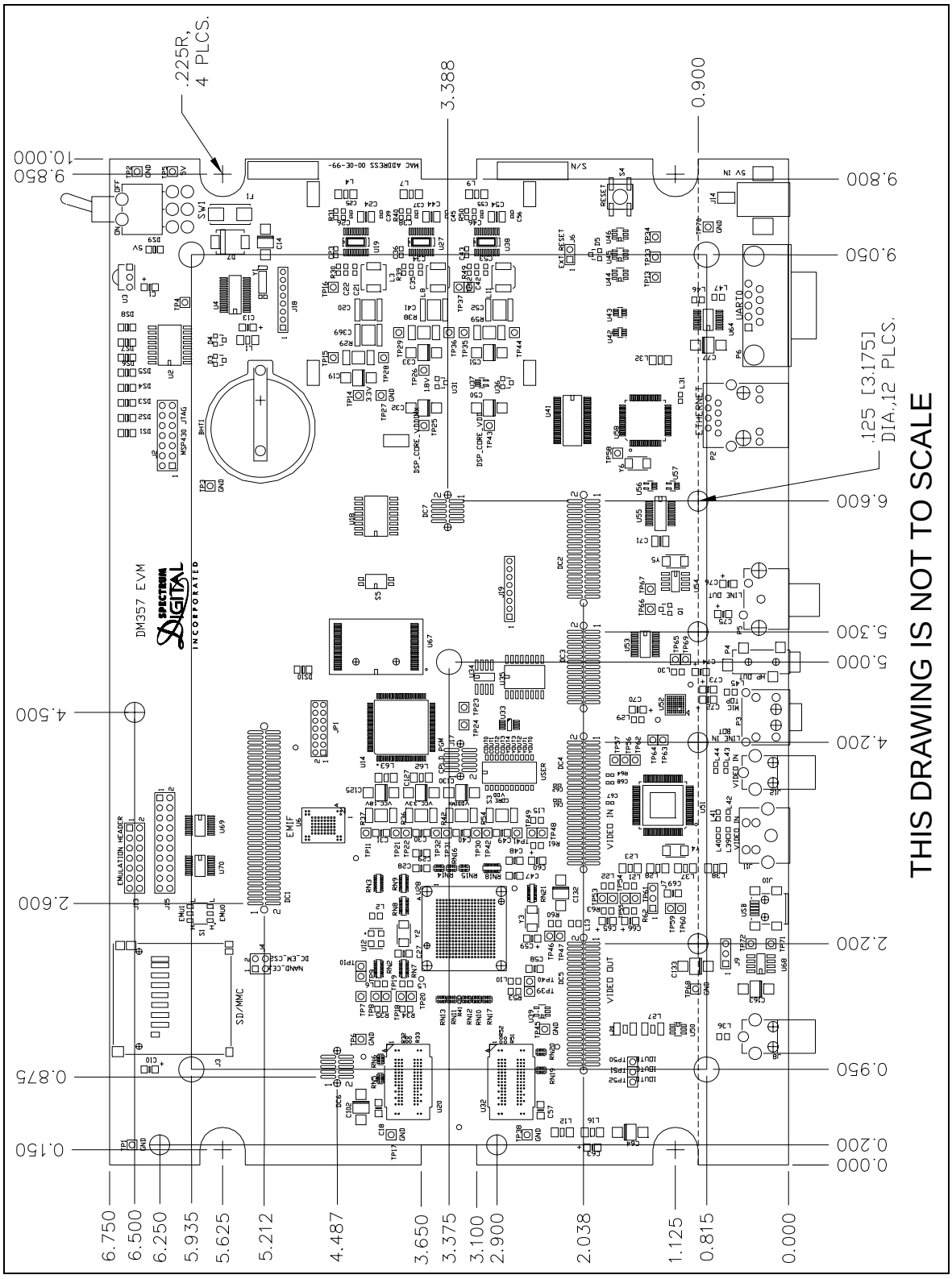
CORE VOLTAGE SUPPORT FOR 0.95 TO 1.2 VOLTS
1.2V -> 28.0K 1%
1.05V -> 56.0K 1%
0.95V -> 118K 1%
Sets Voltage
Connect at pin 1
3.3 sq in AGND, min thermal pad
TPS54310PWP
BLM41P750SPT
UMC2N
HEADER 5X2
VCC_5V
VCC_1.8V
VCC_3.3V
CORE_SUPPLY
CORE_VDD
CORE_VDDMX
1V8_PWR_OK
1V2_PWR_OK
3V3_PWR_OK
VDDMX_EN

Appendix B

Mechanical Information

This appendix contains the mechanical information about the DM357 EVM produced by Spectrum Digital.


.225R,
4 PLCS.
3.388
0.900
.125 [3.175]
DIA.,12 PLCS.
THIS DRAWING IS NOT TO SCALE
DM357 EVM
SPECTRUM DIGITAL INCORPORATED
10.000
9.850
9.800
9.050
6.600
5.300
5.000
4.500
4.200
2.600
2.200
0.875
0.950
0.150
0.200
0.000
6.750
6.500
6.250
5.935
5.625
5.212
4.487
3.650
3.375
3.100
2.900
2.038
1.125
0.815
0.000

[redacted]

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