# MIC38150

## HELDO®
## 1.5A High Efficiency Low Dropout Regulator

## General Description

The MIC38150 is a 1.5A continuous output current step down converter. This is a follow on product in the new HELDO® (High Efficiency Low DropOut Regulators) family, that provide the benefits of an LDO with respect to ease of use, fast transient performance, high PSRR and low noise while offering the efficiency of a switching regulator.

As output voltages move lower, the output noise and transient response of a switching regulator become an increasing challenge for designers. By combining a switcher whose output is slaved to the input of a high performance LDO, high efficiency is achieved with a clean low noise output. The MIC38150 is designed to provide less than 5mV of peak-to-peak noise and over 70dB of PSRR at 1kHz. Furthermore, the architecture of the MIC38150 is optimized for fast load transients allowing the output to maintain less than 30mV of output voltage deviation even during ultra fast load steps. This makes the MIC38150 an ideal choice for low voltage ASICs and other digital ICs.

The MIC38150 features a fully integrated switching regulator and LDO combination, operates with input voltages from 3.0V to 5.5V input and offers adjustable output voltages down to 1.0V.

The MIC38150 is offered in the small 28-pin 4mm × 6mm × 0.9mm MLF® package and can operate from –40°C to +125°C.

Data sheets and support documentation can be found on Micrel's web site at: www.micrel.com

HELDO®

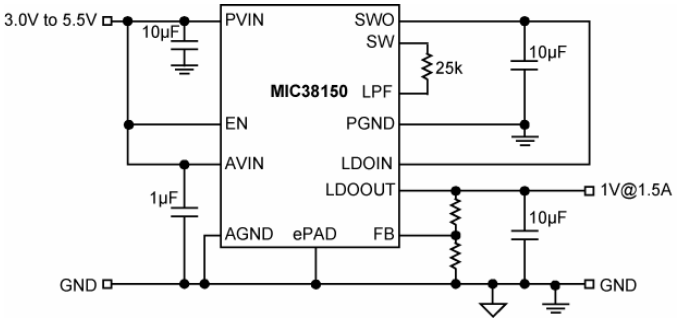
## Features

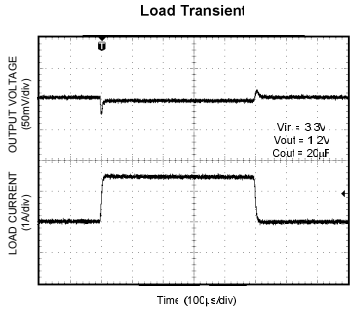
- Output current up to 1.5A
- Input voltage range: 3.0V to 5.5V
- Adjustable output voltage down to 1.0V
- Output noise less than 5mV
- Ultra fast transient performance
- Unique switcher plus LDO architecture
- Fully integrated MOSFET switches
- Micro-power shutdown
- Easy upgrade from LDO as power dissipation becomes an issue
- Thermal shutdown and current limit protection
- 4mm × 6mm × 0.9mm MLF® package

## Applications

- Point-of-load applications
- Networking, server, industrial power
- Wireless base-stations
- Sensitive RF applications

## Typical Application

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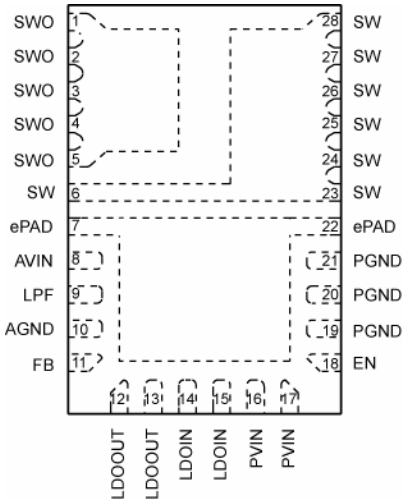
MLF and *Micro*LeadFrame are registered trademark of Amkor Technologies

## Ordering Information

| Part Number | Output Current | Voltage[1] | Junction Temperature Range | Package |
|---|---|---|---|---|
| MIC38150HYHL | 1.5A | ADJ | -40°C to +125°C | PB-Free 28-Pin 4x6 MLF® |

**Note**: For additional voltage options, contact Micrel.

## Pin Configuration




**28-Pin 4mm x 6mm MLF® (ML)**
**(Top View)**

## Pin Description

| Pin Number | Pin Name | Pin Name |
|---|---|---|
| 1, 2, 3, 4, 5 | SWO | Switch (Output): This is the output of the PFM Switcher. |
| 6, 23, 24, 25, 26, 27, 28 | SW | Switch Node: Attach external resistor from LPF to increase hysteretic frequency. |
| 7, 22 | ePAD | Exposed heat-sink pad. Connect externally to PGND. |
| 8 | AVIN | Analog Supply Voltage: Supply for the analog control circuitry. Requires bypass capacitor to ground. Nominal bypass capacitor is 1µF. |
| 9 | LPF | Low Pass Filter: Attach external resistor from SW to increase hysteretic frequency. |
| 10 | AGND | Analog Ground. |
| 11 | FB | Feedback: Input to the error amplifier. Connect to the external resistor divider network to set the output voltage. |
| 12, 13 | LDOOUT | LDO Output: Output of voltage regulator. Place capacitor to ground to bypass the output voltage. Nominal bypass capacitor is 10µF. |
| 14, 15 | LDOIN | LDO Input: Connect to SW output. Requires a bypass capacitor to ground. Nominal bypass capacitor is 10µF. |
| 16, 17 | PVIN | Input Supply Voltage (Input): Requires bypass capacitor to GND. Nominal bypass capacitor is 10µF. |
| 18 | EN | Enable (Input): Logic low will shut down the device, reducing the quiescent current to less than 50µA. This pin can also be used as an under-voltage lockout function by connecting a resistor divider from EN pin-to-VIN and GND. It should be not left open. |
| 19, 20, 21 | PGND | Power Ground. |

## Absolute Maximum Ratings[1]

Supply Voltage ($V_{IN}$) ..... 6V
Output Switch Voltage ($V_{SW}$) ..... 6V
Logic Input Voltage ($V_{EN}$) ..... -0.3V to VIN
Power Dissipation ..... Internally Limited[3]
Storage Temperature ($T_S$) ..... -65°C ≤ $T_J$ ≤ +150°C
Lead Temperature (soldering, 10sec) ..... 260°C
ESD Rating[4] ..... 1.5kV

## Operating Ratings[2]

Supply voltage ($V_{IN}$) ..... 3.0V to 5.5V
Enable Input Voltage ($V_{EN}$) ..... 0V to $V_{IN}$
Junction Temperature Range ..... –40°C ≤ $T_J$ ≤ +125°C
Package Thermal Resistance
4mm × 6mm MLF-28 ($\theta_{JA}$) ..... 24°C/W

## Electrical Characteristics[5]

$T_A$ = 25°C with $V_{IN}$ = $V_{EN}$ = 5V; $I_{OUT}$ = 10mA, $V_{OUT}$ = 1.8V. **Bold** values indicate –40°C ≤ $T_J$ ≤ +125°C, unless noted.

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Supply Voltage Range | | **3.0** | | **5.5** | V |
| Under-Voltage Lockout Threshold | Turn-on | | 2.85 | | V |
| UVLO Hysteresis | | | 100 | | mV |
| Quiescent Current | $I_{OUT}$ = 0A, Not switching, Open Loop | | 1 | | mA |
| Turn-on Time | $V_{OUT}$ to 95% of nominal | | 200 | 500 | µs |
| Shutdown Current | $V_{EN}$ = 0V | | 30 | **50** | µA |
| Feedback Voltage | ±2.5% | **0.975** | 1 | **1.025** | V |
| Feedback Current | | | 5 | | nA |
| Dropout Voltage ($V_{IN}$ – $V_{OUT}$) | $I_{LOAD}$ = 1.5A; $V_{OUT}$ = 3V | | 0.85 | **1.2** | V |
| Current Limit | $V_{FB}$ = 0.9×$V_{NOM}$ | **1.75** | 3 | | A |
| Output Voltage Load Regulation | $V_{OUT}$ = 1.8V, 10mA to 1.5A | | 0.1 | 1 | % |
| Output Voltage Line Regulation | $V_{OUT}$ = 1.8V, $V_{IN}$ from 3.0V to 5.5V | | 0.35 | 0.5 | %/V |
| Output Ripple | $I_{LOAD}$ = 1.5A, $C_{OUTLDO}$ = 20µF, $C_{OUTSW}$ = 20µF LPF=25kΩ | | 2 | | mV |
| Over-Temperature Shutdown | | | 150 | | °C |
| Over-Temperature Shutdown Hysteresis | | | 15 | | °C |
| **Enable Input[6]** | | | | | |
| Enable Input Threshold | Regulator enable | **0.90** | 1 | **1.1** | V |
| Enable Hysteresis | | **20** | 100 | **200** | mV |
| Enable Input Current | | | 0.03 | 1 | µA |

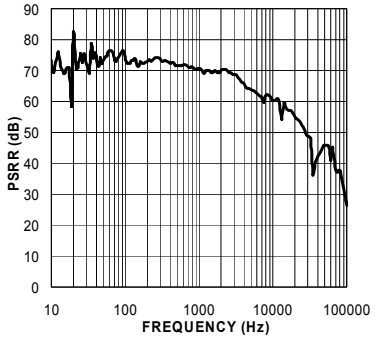
**Notes:**

1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating.
3. The maximum allowable power dissipation of any $T_A$ (ambient temperature) is $P_{D(max)} = (T_{J(max)} – T_A) / \theta_{JA}$. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the regulator will go into thermal shutdown.
4. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5k in series with 100pF.
5. Specification for packaged product only.
6. Enable pin should not be left open.

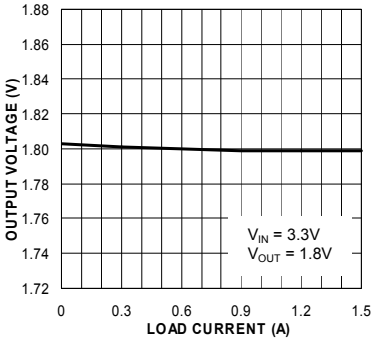
## Typical Characteristics

$V_{IN}$ = 3.3V, $V_{OUT}$ = 1.8V, $C_{OUT}$ = 10µF, $R_{LPF}$ = 25kΩ, $I_{OUT}$ = 100mA, unless noted

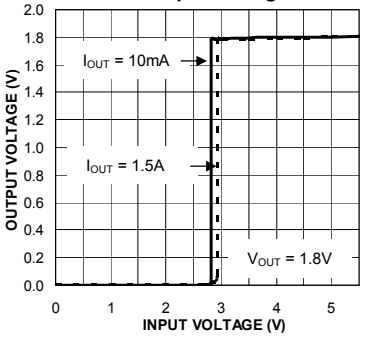
**MIC38150 PSRR**



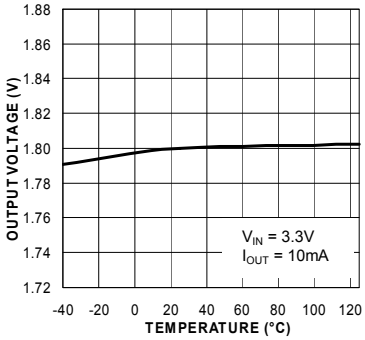

**Load Regulation**



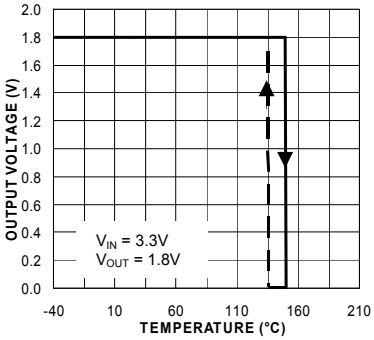

**Output Voltage vs. Input Voltage**



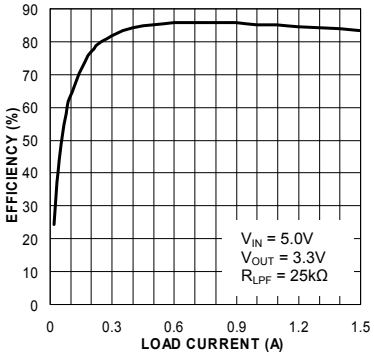

**Output Voltage vs. Temperature**



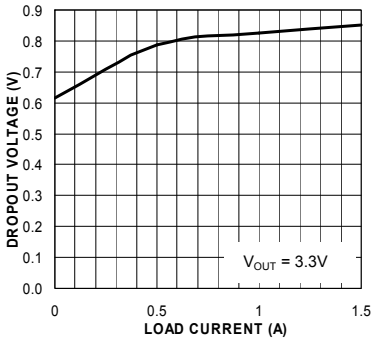

**Thermal Shutdown**



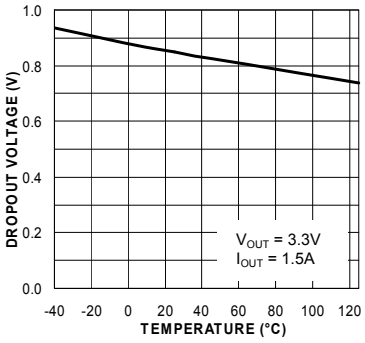

**MIC38150 Efficiency**



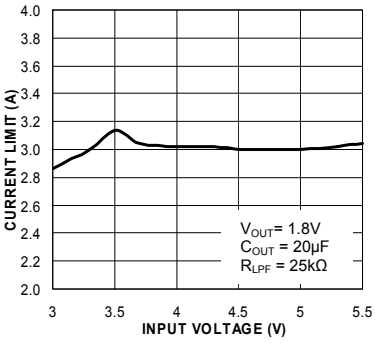

**Dropout Voltage vs. Load Current**



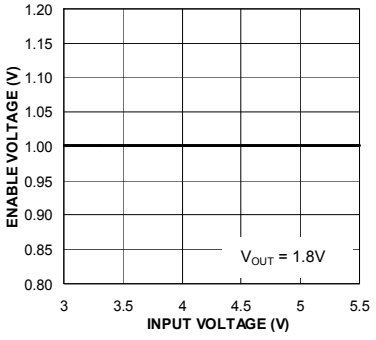

**Dropout Voltage vs. Temperature**



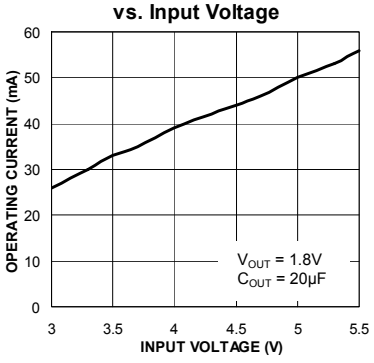

**Current Limit vs. Input Voltage**




**Enable Threshold**



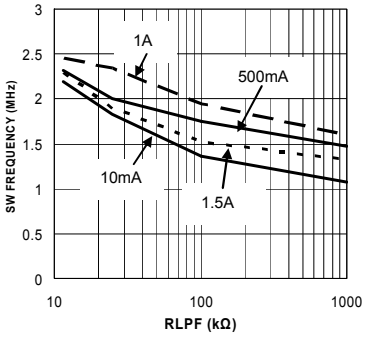

**Operating Current vs. Input Voltage**



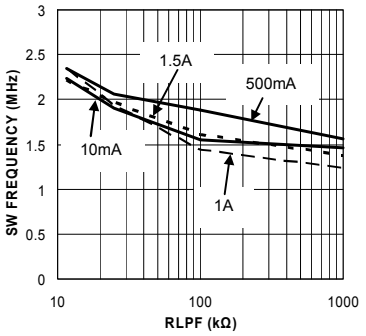
## Typical Characteristics

$V_{IN}$ = 3.3V, $V_{OUT}$ = 1.8V, $C_{OUT}$ = 10µF, $R_{LPF}$ = 25kΩ, $I_{OUT}$ = 100mA, unless noted

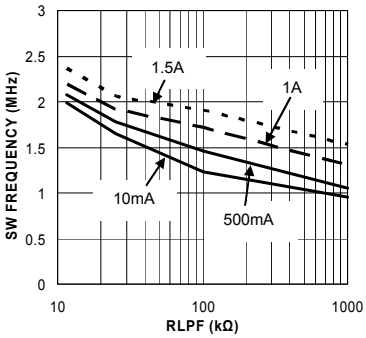
**Switch Frequency vs. RLPF Resistance (3.3V-1.0V)**



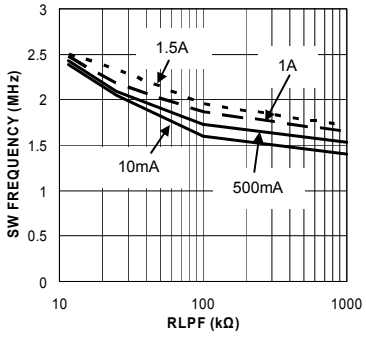

**Switch Frequency vs. RLPF Resistance (3.3V-1.8V)**



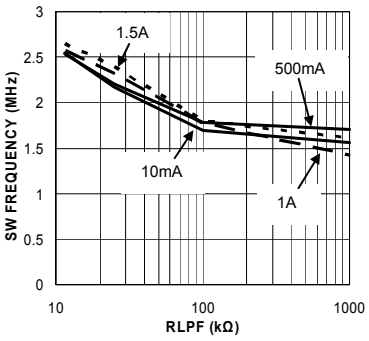

**Switch Frequency vs. RLPF Resistance (5.0V-1.0V)**




**Switch Frequency vs. RLPF Resistance (5.0V-1.8V)**



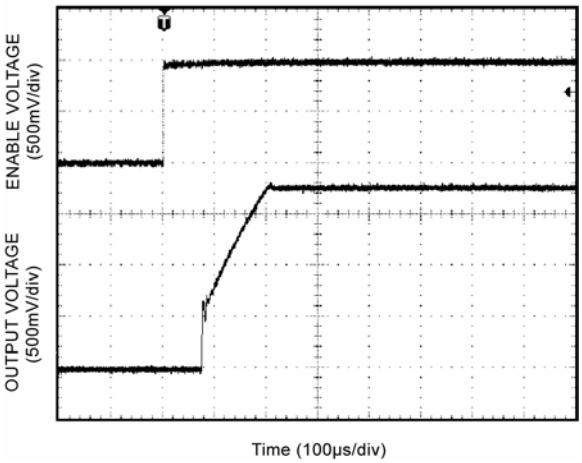

**Switch Frequency vs. RLPF Resistance (5.0V-2.5V)**



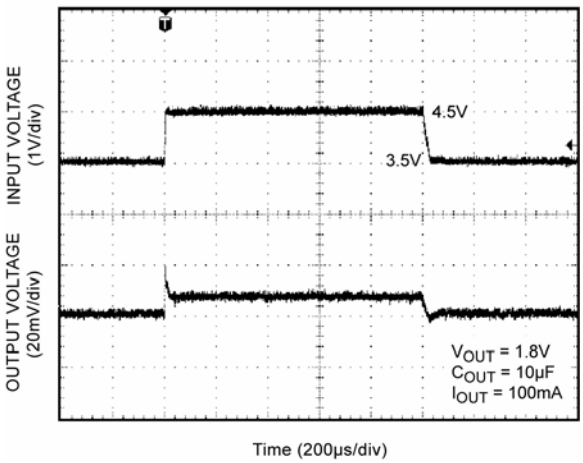
## Functional Characteristics

$V_{IN}$ = 3.3V, $V_{OUT}$ = 1.8V, $C_{OUT}$ = 10µF, Inductor = 470nH; $R_{LPF}$ = 25kΩ, $I_{OUT}$ = 100mA, unless noted

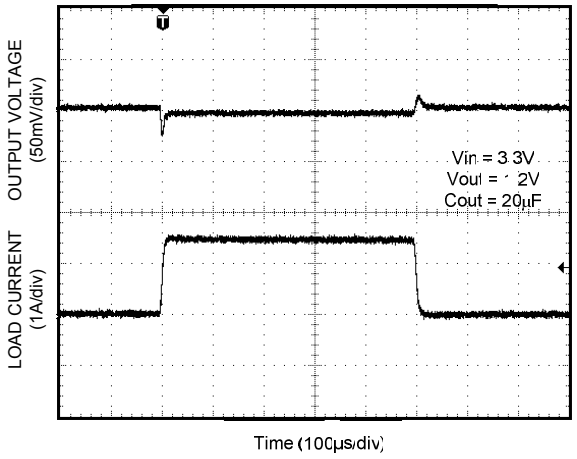
**Enable Turn-On**



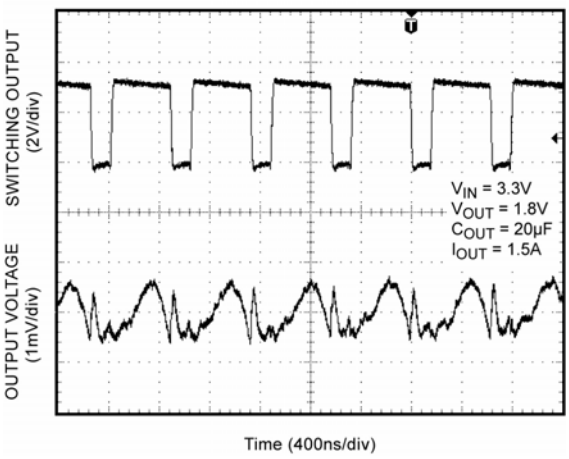

**Line Transient**




**Load Transient**

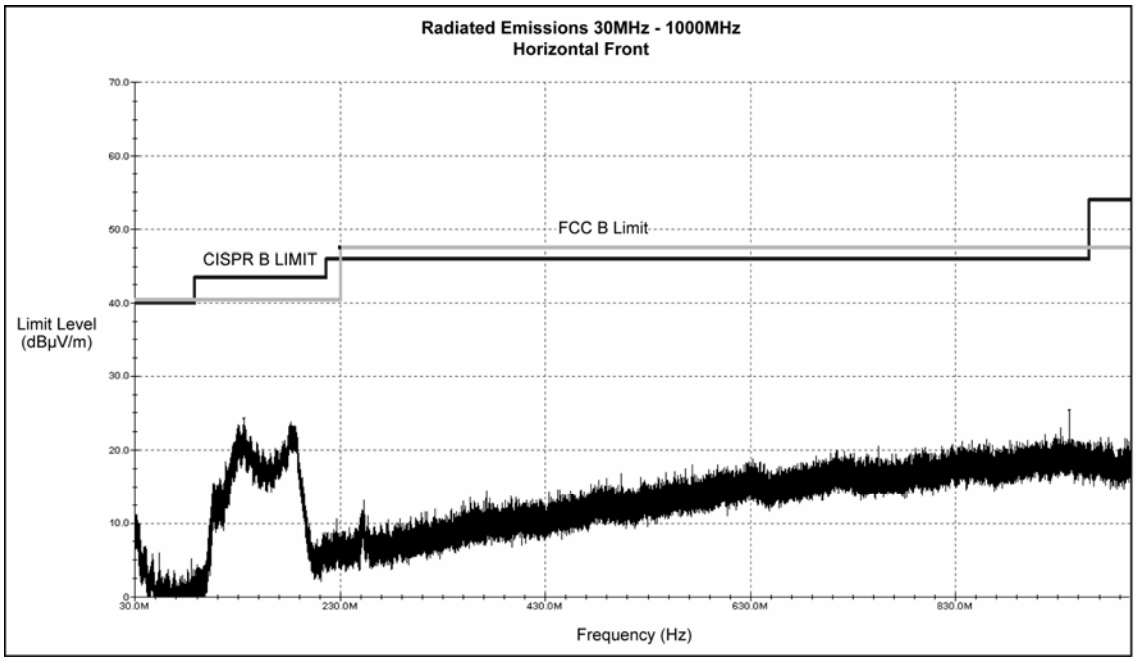



**Output Ripple**

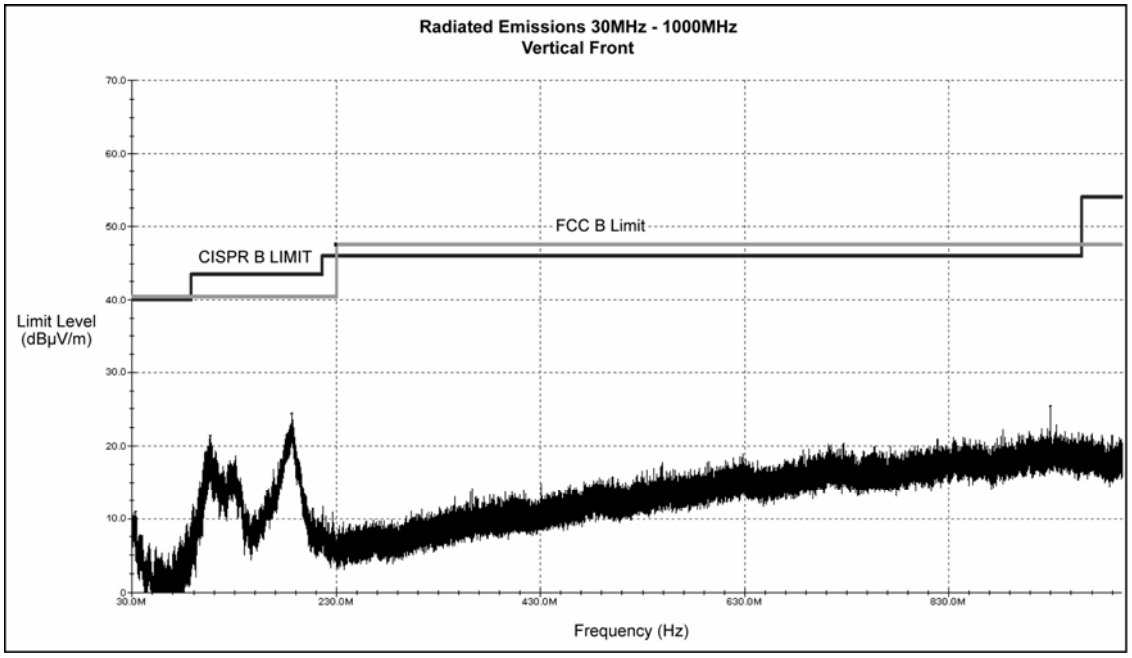


## EMI Performance

$V_{OUT}$ =1.8V, $I_{OUT}$ =1.2A




**EMI Test – Horizontal Front**

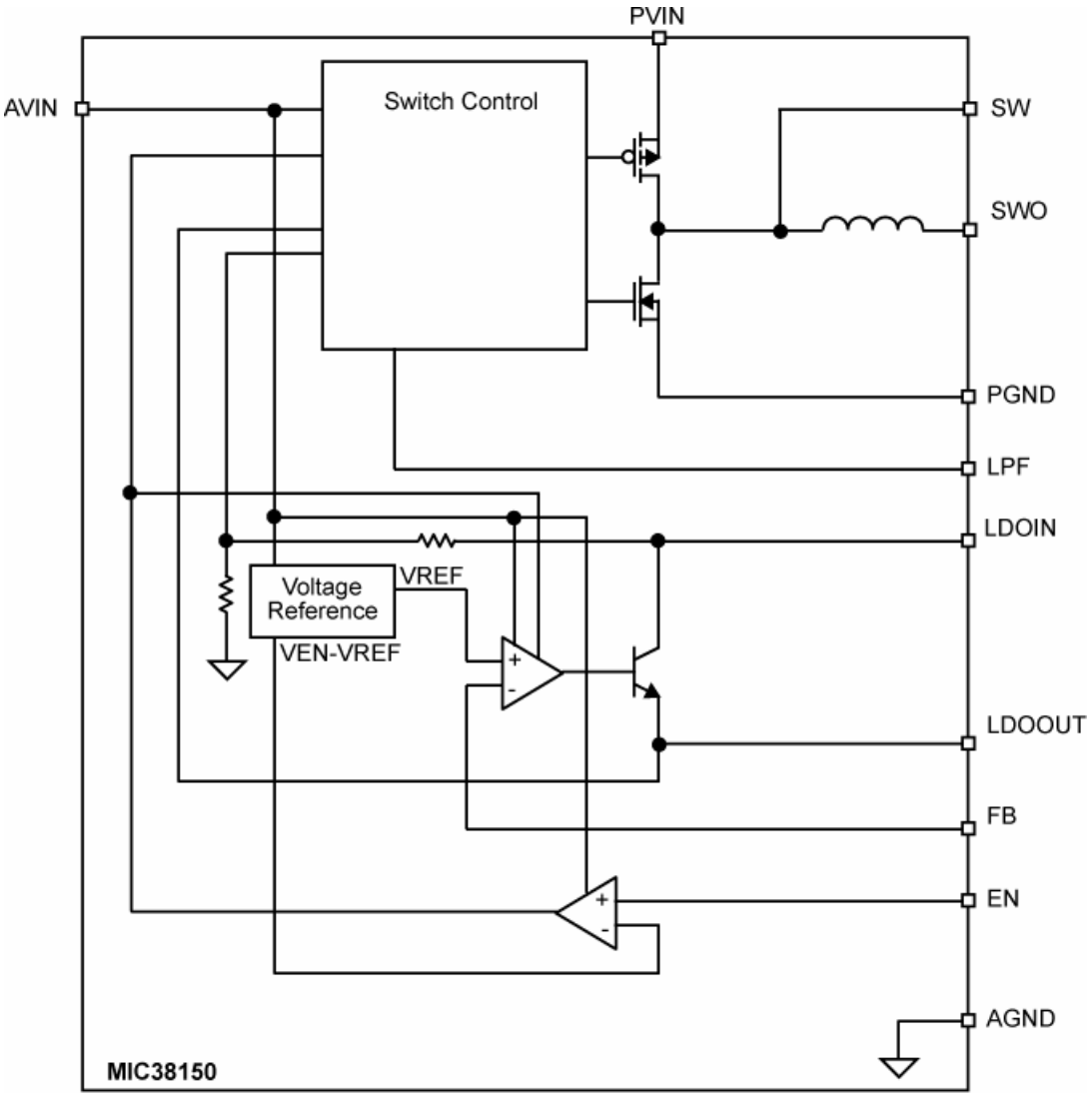



**EMI Test – Vertical Front**

**Additional components to MIC38150 Evaluation Board:**

1. Input Ferrite Bead Inductor. Part number: BLM21AG102SN1D
2. 0.1µF and 0.01µF ceramic bypass capacitors on PVIN, SW, SWO, and LDOOUT pins.

## Block Diagram



## Application Information

### Enable Input

The MIC38150 features a TTL/CMOS compatible positive logic enable input for on/off control of the device. High enables the regulator while low disables the regulator. In shutdown the regulator consumes very little current (only a few microamperes of leakage). For simple applications the enable (EN) can be connected to $V_{IN}$ (IN).

### Input Capacitor

PVIN provides power to the MOSFETs for the switch mode regulator section and the gate drivers. Due to the high switching speeds, a 10µF capacitor is recommended close to PVIN and the power ground (PGND) pin for bypassing.

Analog $V_{IN}$ (AVIN) provides power to the analog supply circuitry. AVIN and PVIN must be tied together externally. Careful layout should be considered to ensure high frequency switching noise caused by PVIN is reduced before reaching AVIN. A 1µF capacitor as close to AVIN as possible is recommended.

### Output Capacitor

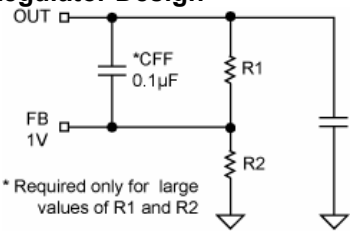
The MIC38150 requires an output capacitor for stable operation. As a µCap LDO, the MIC38150 can operate with ceramic output capacitors of 10µF or greater. Values of greater than 10µF improve transient response and noise reduction at high frequency. X7R/X5R dielectric-type ceramic capacitors are recommended because of their superior temperature performance. X7R-type capacitors change capacitance by 15% over their operating temperature range and are the most stable type of ceramic capacitors. Larger output capacitances can be achieved by placing tantalum or aluminum electrolytics in parallel with the ceramic capacitor. For example, a 100µF electrolytic in parallel with a 10µF ceramic can provide the transient and high frequency noise performance of a 100µF ceramic at a significantly lower cost. Specific undershoot/overshoot performance will depend on both the values and ESR/ESL of the capacitors.

For less than 5mV noise performance at higher current loads, 20µF capacitors are recommended at LDOIN and LDOOUT.

### Low Pass Filter Pin

The MIC38150 features a Low Pass Filter (LPF) pin for adjusting the switcher frequency. By tuning the frequency, the user can further improve output ripple. Adjusting the frequency is accomplished by connecting a resistor between the LPF and SW pins. A small value resistor would increase the frequency while a larger value resistor decreases the frequency. Recommended $R_{LPF}$ value is 25kΩ.

### Adjustable Regulator Design




**Adjustable Regulator with Resistors**

The adjustable MIC38150 output voltage can be programmed from 1V to 5.0V using a resistor divider from output to the FB pin. Resistors can be quite large, up to 100kΩ because of the very high input impedance and low bias current of the sense amplifier. For large value resistors (>50kΩ), R1 should be bypassed by a small capacitor ($C_{FF}$ = 0.1µF bypass capacitor) to avoid instability due to phase lag at the ADJ/SNS input.

The output resistor divider values are calculated by:

$$V_{OUT} = 1V \times (\frac{R1}{R2} + 1)$$

### Efficiency Considerations

Efficiency is defined as the amount of useful output power, divided by the amount of power supplied.

$$\text{Efficiency}(\%) = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}} \times 100$$

Maintaining high efficiency serves two purposes. It reduces power dissipation in the power supply, reducing the need for heat sinks and thermal design considerations and it reduces consumption of current for battery powered applications. Reduced current draw from a battery increases the devices operating time and is critical in hand held devices.

There are two types of losses in switching converters; DC losses and switching losses. DC losses are simply the power dissipation of $I^2R$. Power is dissipated in the high side switch during the on cycle. Power loss is equal to the high side MOSFET $R_{DSON}$ multiplied by the Switch Current$^2$. During the off cycle, the low side N-channel MOSFET conducts, also dissipating power. Device operating current also reduces efficiency. The product of the quiescent (operating) current and the supply voltage is another DC loss.

Over 100mA, efficiency loss is dominated by MOSFET $R_{DSON}$ and inductor losses. Higher input supply voltages will increase the Gate to Source threshold on the internal MOSFETs, reducing the internal $RD_{DSON}$. This improves efficiency by reducing DC losses in the device. As the inductors are reduced in size, the inductor losses are mainly caused by the DC resistance (DCR).

The DCR losses can be calculated as follows:

$$L\_P_D = I_{OUT}^2 \times DCR$$

Efficiency loss due to DCR is minimal at light loads and gains significance as the load is increased.

## PCB Layout Guideline

**Warning!!! To minimize EMI and output noise, follow these layout recommendations.**

PCB Layout is critical to achieve reliable, stable and efficient performance. A ground plane is required to control EMI and minimize the inductance in power, signal and return paths.

The following guidelines should be followed to insure proper operation of the MIC38150.

**IC**

- Place the IC close to the point of load (POL).
- Use fat traces to route the input and output power lines.
- The exposed pad (ePAD) on the bottom of the IC must be connected to the PGND pins of the IC.
- Use several vias to connect the ePAD to the ground plane.
- Signal and power grounds should be kept separate and connected at only one location.
- Keep the switch node (SW) away from the feedback (FB) pin.

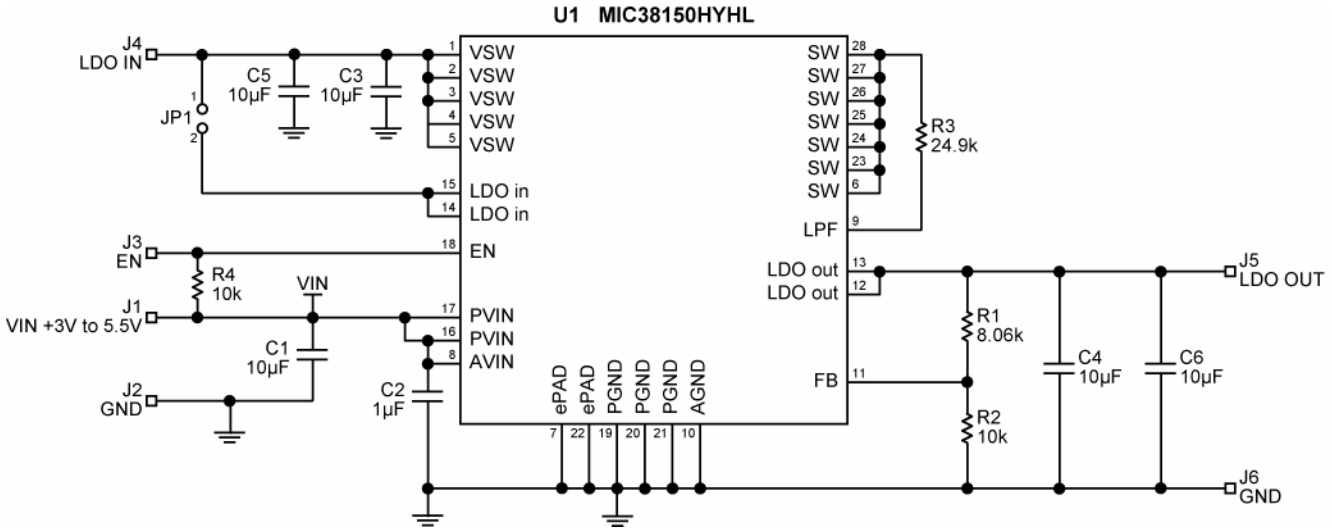
**Input Capacitor**

- Place the input capacitor next.
- Place the input capacitors on the same side of the board and as close to the MIC38150 as possible.
- Keep both the PVIN and PGND connections short.
- Place several vias to the ground plane close to the input capacitor ground terminal, but not between the input capacitors and IC pins.
- Use either X7R or X5R dielectric input capacitors. Do not use Y5V or Z5U type capacitors.
- Do not replace the ceramic input capacitor with any other type of capacitor. Any type of capacitor can be placed in parallel with the input capacitor.
- If a Tantalum input capacitor is placed in parallel with the input capacitor, it must be recommended for switching regulator applications and the operating voltage must be derated by 50%.
- In “Hot-Plug” applications, a Tantalum or Electrolytic bypass capacitor must be used to limit the over-voltage spike seen on the input supply with power is suddenly applied.
- The 1µF capacitor, which connects to the AVIN terminal, must be located right at the IC. The AVIN terminal is very noise sensitive and placement of the capacitor is very critical. Connections must be made with wide trace.

**Output Capacitor**

- Use a wide trace to connect the VSW output capacitor ground terminal to the PVIN input capacitor ground terminal.
- The feedback trace should be separate from the power trace and connected as close as possible to the output capacitor.

## Evaluation Board Schematics



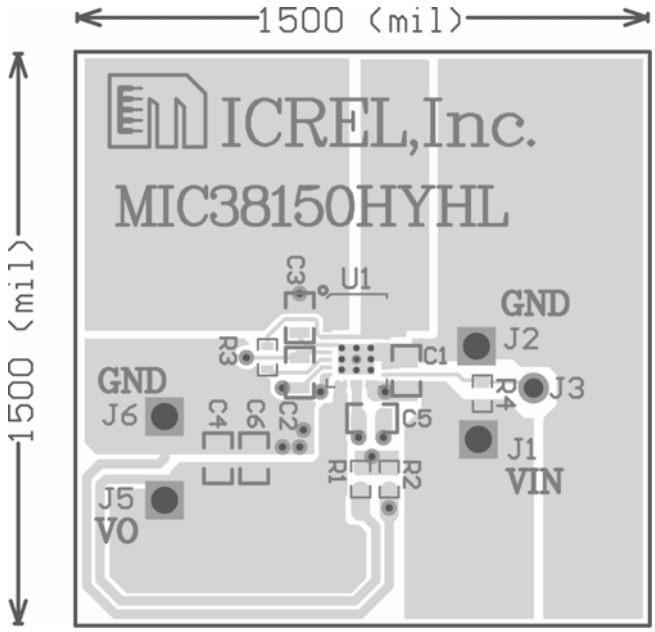

## Bill of Materials

| Item | Part Number | Manufacturer | Description | Qty |
|---|---|---|---|---|
| C1, C3, C4, C5, C6 | 0805ZD106MAT2A | AVX[1] | 10uF, 10V, X5R, 0805 Ceramic Capacitor | 5 |
| | LMK212BJ106KG-T | Taiyo Yuden[2] | | |
| | C2012X5R1A106K | TDK[3] | | |
| | GRM219R61A106KE44D | Murata[4] | | |
| C2 | C2012X5R1A105K | TDK[3] | 1uF, 10V, X5R, 0805 Ceramic Capacitor | 1 |
| | 0805ZD105KAT2A | AVX[1] | | |
| | GRM219R61A105MA01D | Murata[4] | | |
| R1 | CRCW06038061FRT1 | Vishay[5] | 8.06k, 1%, 1/10W, 0603 | 1 |
| R2, R4 | CRCW06031002KEYE3 | Vishay[5] | 10k, 1%, 1/10W, 0603 | 2 |
| R3 | CRCW06032492FRT1 | Vishay[5] | 24.9k, 1%, 1/10W, 0603 | 1 |
| **U1** | **MIC38150-HYHL** | **Micrel, Inc.[6]** | **HELDO® 1.5A High Efficiency Low Dropout Regulator** | **1** |

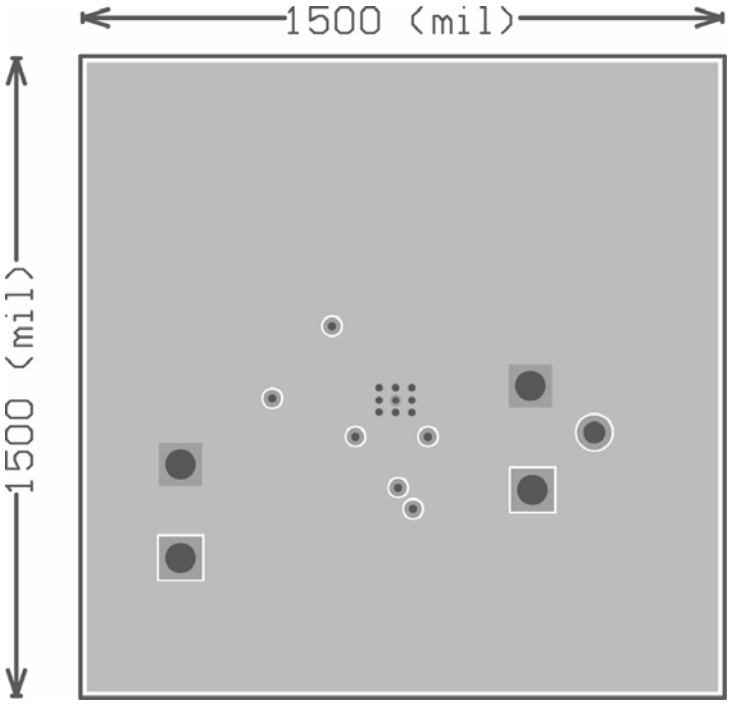
**Notes**:

1. AVX: www.avx.com
2. Taiyo Yuden: www.t-yuden.com
3. TDK: www.tdk.com
4. Murata: www.murata.com
5. Vishay: www.vishay.com
6. **Micrel, Inc.: www.micrel.com**

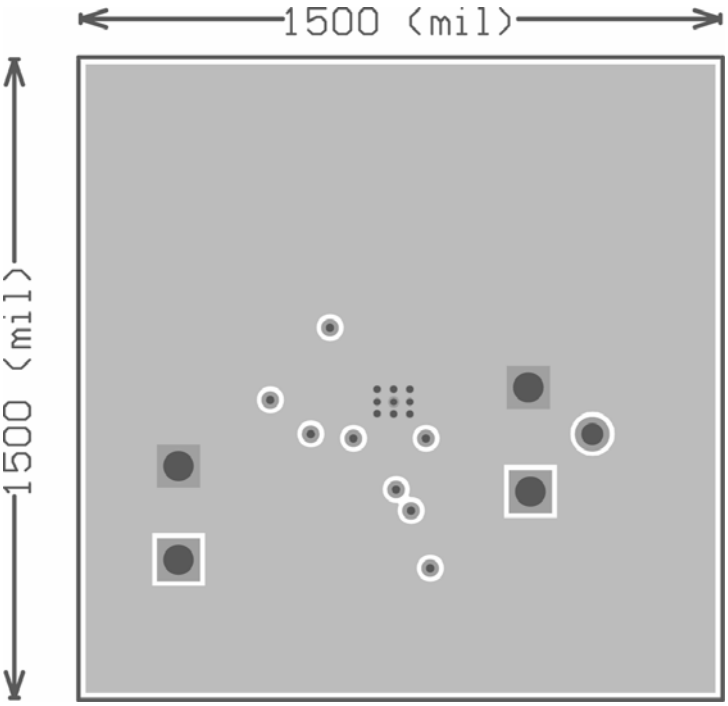
## PCB Layout



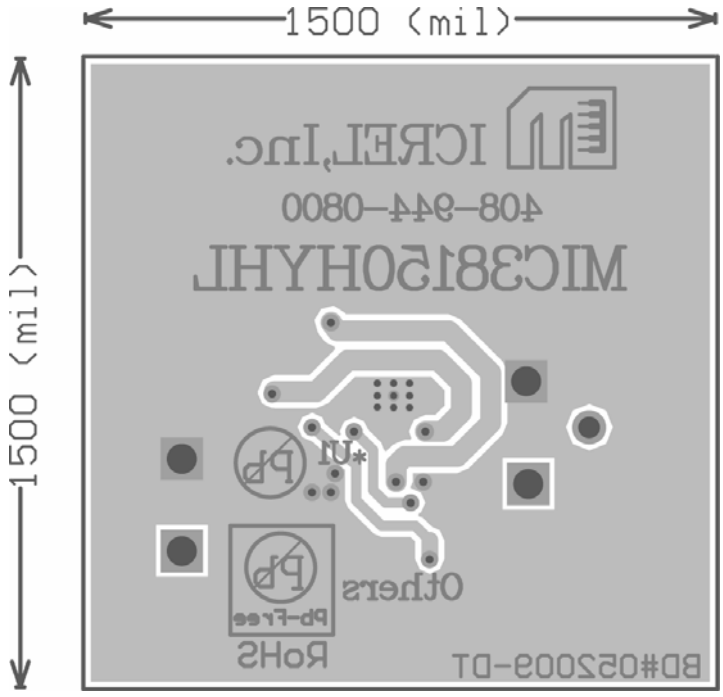

**Top Layer**




Mid Layer 1

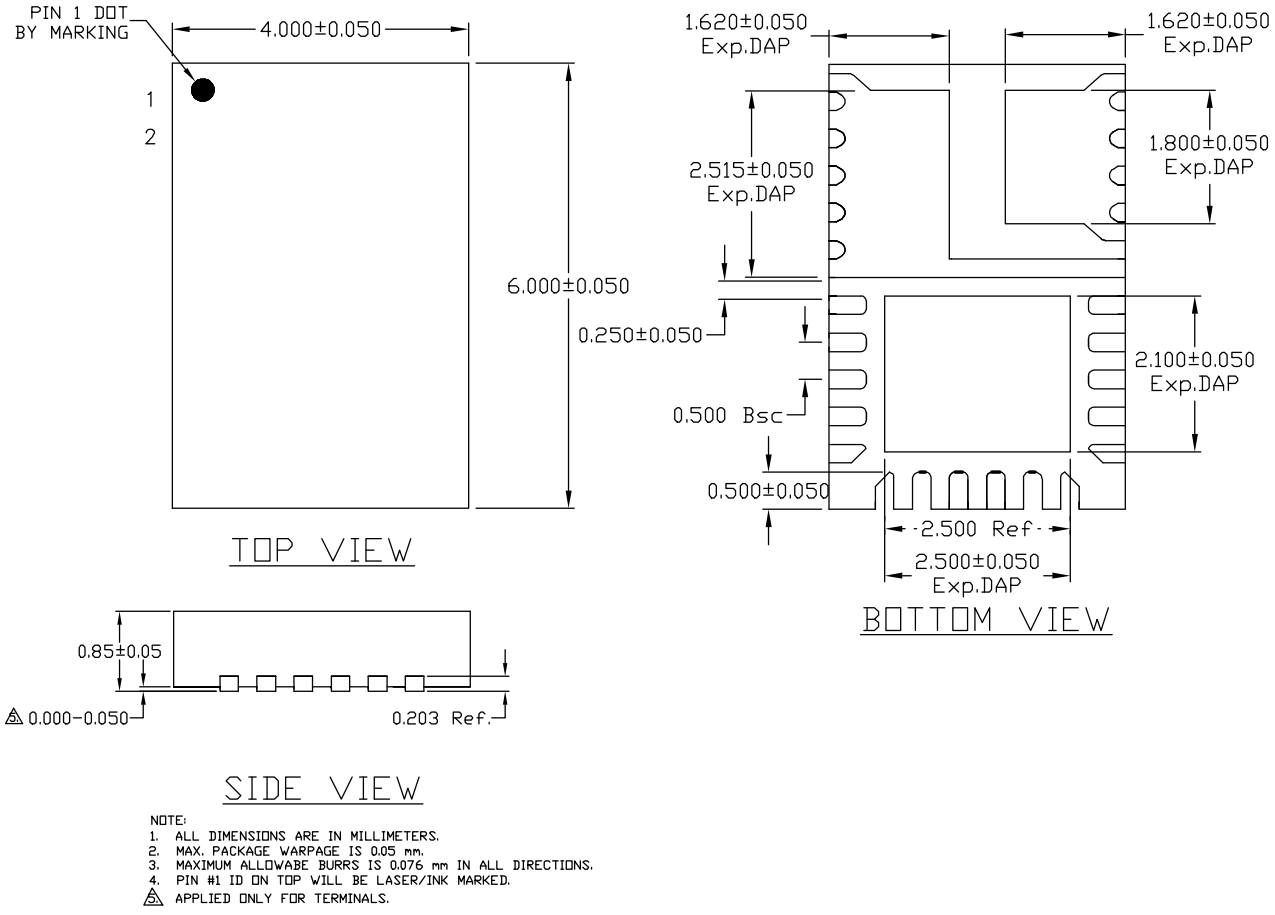



Mid Layer 2




**Bottom Layer**

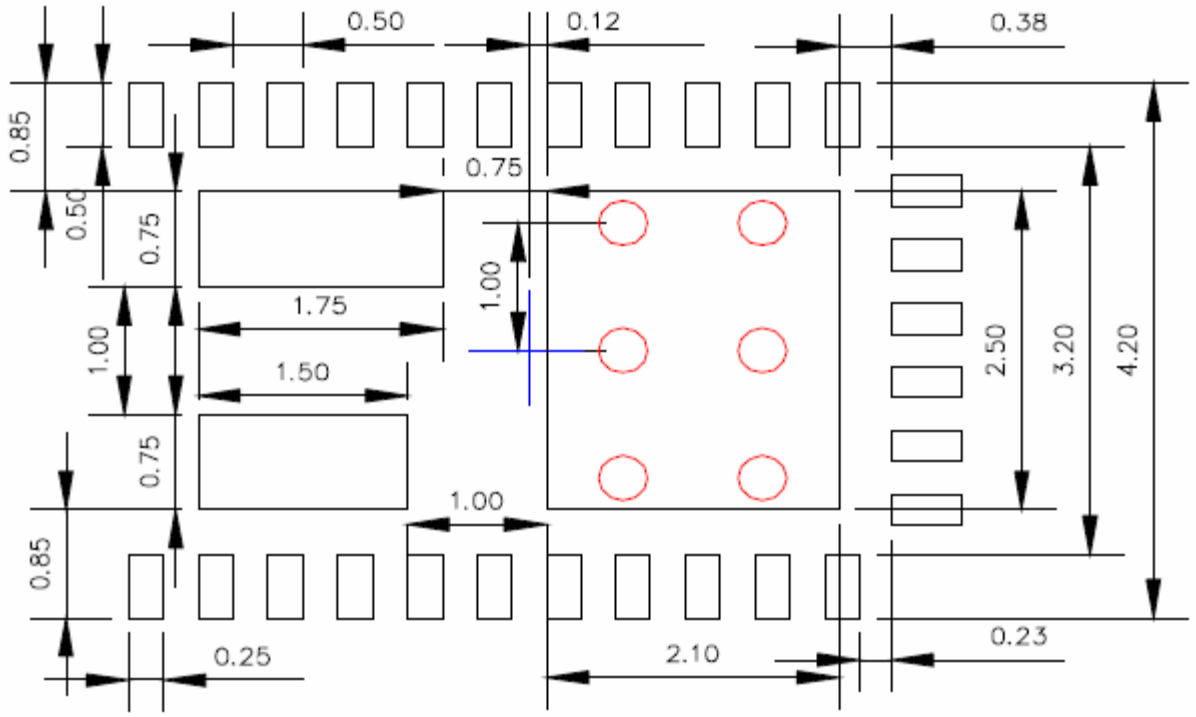
## Package Information




**28-Pin 4mm x 6mm MLF® (ML)**

## Recommended Landing Pattern

LP # HMLF46T-28LD-LP-1
All units are in mm
Tolerance ± 0.05 if not noted




Red circle indicates Thermal Via. Size should be .300-.350 mm in diameter and it should be connected to GND plane for maximum thermal performance.

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