NTPF082N65S3F

Power MOSFET, N-Channel, SUPERFET® III, FRFET®, 650 V, 40 A, 82 mΩ

ON Semiconductor®

www.onsemi.com

V_{DS}	$R_{DS(ON)}$ MAX	I_D MAX
650 V	82 mΩ @ 10 V	40 A

Description

SUPERFET III MOSFET is ON Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate.

Consequently, SUPERFET III MOSFET is very suitable for the various power system for miniaturization and higher efficiency.

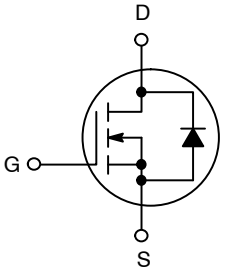
SUPERFET III FRFET MOSFET's optimized reverse recovery performance of body diode can remove additional component and improve system reliability.

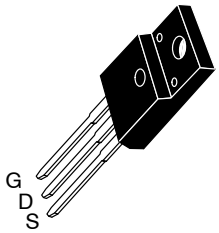
Features

- 700 V @ T_J = 150°C
- Typ. $R_{DS(on)}$ = 70 mΩ
- Ultra Low Gate Charge (Typ. Q_g = 70 nC)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)}$ = 680 pF)
- 100% Avalanche Tested
- These Devices are Pb−Free and are RoHS Compliant

Applications

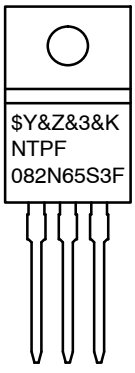
- Telecom/Sever Power Supplies
- Industrial Power Supplies
- UPS/Solar





TO−220 FULLPAK
CASE 221D

MARKING DIAGAM



$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= Numeric Date Code
&K	= Lot Code
NTPF082N65S3F	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, Unless otherwise specified)

Symbol	Parameter		Value	Unit
V_{DSS}	Drain to Source Voltage		650	V
V_{GSS}	Gate to Source Voltage	DC	±30	V
		AC (f > 1 Hz)	±30	V
I_D	Drain Current	Continuous (T_C = 25°C)	40*	A
		Continuous (T_C = 100°C)	25.5*	
I_{DM}	Drain Current	Pulsed (Note 1)	100*	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		510	mJ
I_{AS}	Avalanche Current (Note 2)		4.8	A
E_{AR}	Repetitive Avalanche Energy (Note 1)		0.48	mJ
dv/dt	MOSFET dv/dt		100	V/ns
	Peak Diode Recovery dv/dt (Note 3)		50	
P_D	Power Dissipation	(T_C = 25°C)	48	W
		Derate Above 25°C	0.38	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		−55 to +150	°C
T_L	Maximum Lead Temperature for Soldering, 1/8″ from Case for 5 s		300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
*Drain current limited by maximum junction temperature.
1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. I_{AS} = 4.8 A, R_G = 25 Ω, starting T_J = 25°C.
3. I_{SD} ≤ 20 A, di/dt ≤ 200 A/μs, V_{DD} ≤ 400 V, starting T_J = 25°C.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	2.62	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Marking	Package	Packing Method	Quantity
NTPF082N65S3F	NTPF082N65S3F	TO−220 FULLPACK (Pb−Free)	Tube	50 Units

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	V_{GS} = 0 V, I_D = 1 mA, T_J = 25°C	650	–	–	V
		V_{GS} = 0 V, I_D = 1 mA, T_J = 150°C	700	–	–	V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	I_D = 10 mA, Referenced to 25°C	–	0.67	–	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 650 V, V_{GS} = 0 V	–	–	10	μA
		V_{DS} = 520 V, T_C = 125°C	–	97	–	
I_{GSS}	Gate to Body Leakage Current	V_{GS} = ±30 V, V_{DS} = 0 V	–	–	±100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 4 mA	3.0	–	5.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 20 A	–	70	82	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 20 V, I_D = 20 A	–	24	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 400 V, V_{GS} = 0 V, f = 1 MHz	–	3240	–	pF
C_{oss}	Output Capacitance		–	70	–	pF
$C_{oss(eff.)}$	Effective Output Capacitance	V_{DS} = 0 V to 400 V, V_{GS} = 0 V	–	680	–	pF
$C_{oss(er.)}$	Energy Related Output Capacitance	V_{DS} = 0 V to 400 V, V_{GS} = 0 V	–	125	–	pF
$Q_{g(tot)}$	Total Gate Charge at 10 V	V_{DS} = 400 V, I_D = 20 A, V_{GS} = 10 V (Note 4)	–	70	–	nC
Q_{gs}	Gate to Source Gate Charge		–	24	–	nC
Q_{gd}	Gate to Drain “Miller” Charge		–	27	–	nC
ESR	Equivalent Series Resistance	f = 1 MHz	–	2.3	–	Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 400 V, I_D = 20 A, V_{GS} = 10 V, R_g = 3 Ω (Note 4)	–	30	–	ns
t_r	Turn-On Rise Time		–	27	–	ns
$t_{d(off)}$	Turn-Off Delay Time		–	64	–	ns
t_f	Turn-Off Fall Time		–	3.7	–	ns
SOURCE-DRAIN DIODE CHARACTERISTICS						
I_S	Maximum Continuous Source to Drain Diode Forward Current		–	–	40	A
I_{SM}	Maximum Pulsed Source to Drain Diode Forward Current		–	–	100	A
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_{SD} = 20 A	–	–	1.3	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_{SD} = 20 A, dI_F/dt = 100 A/μs	–	103	–	ns
Q_{rr}	Reverse Recovery Charge		–	397	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature typical characteristics.

TYPICAL PERFORMANCE CHARACTERISTICS

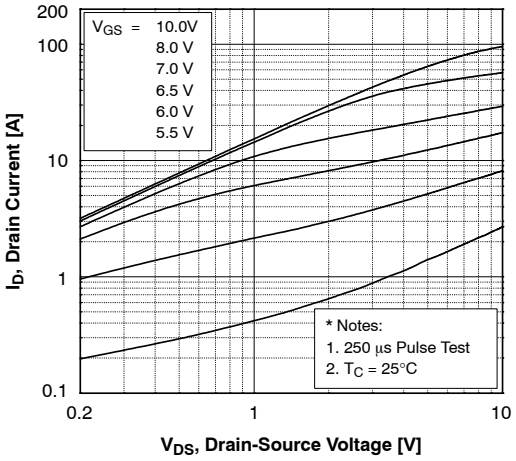


Figure 1. On-Region Characteristics

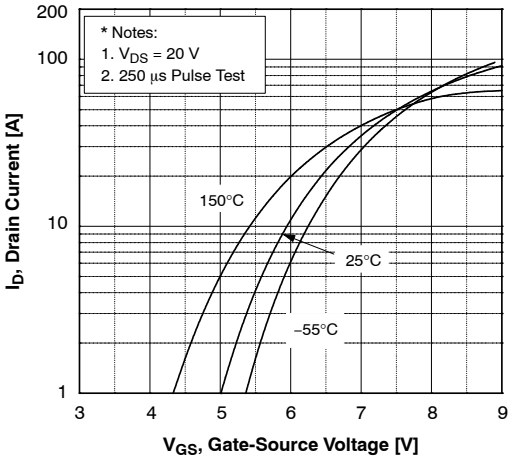


Figure 2. Transfer Characteristics

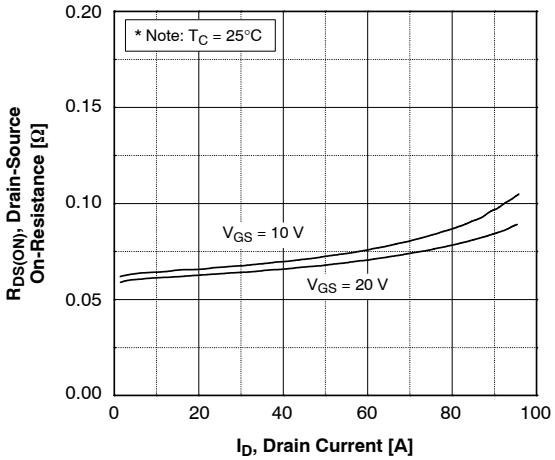


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

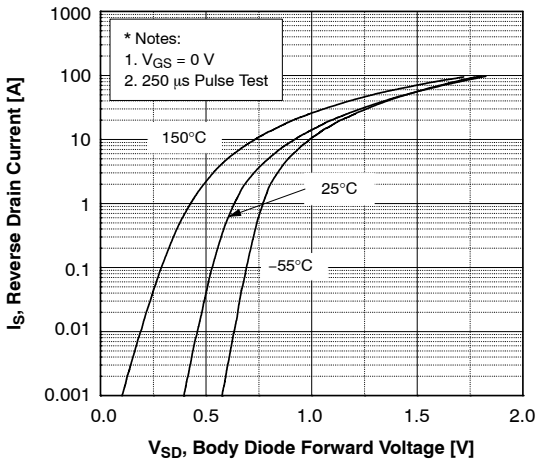


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

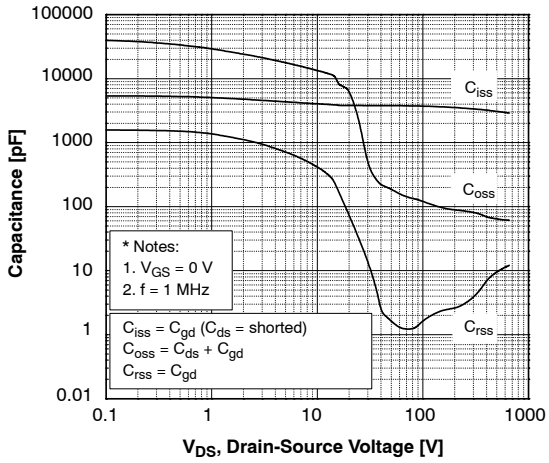


Figure 5. Capacitance Characteristics

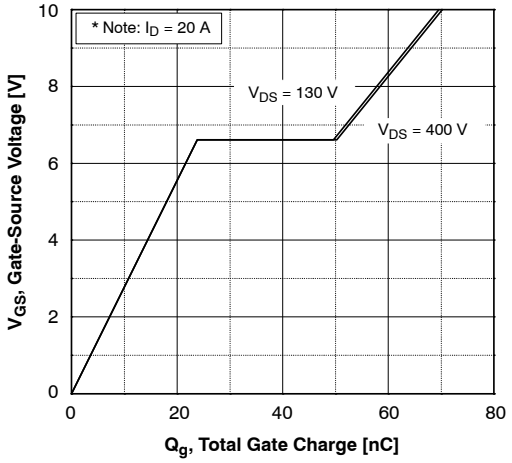


Figure 6. Gate Charge Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

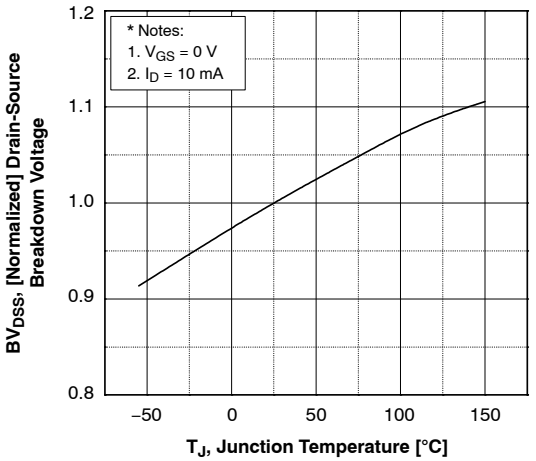


Figure 7. Breakdown Voltage Variation vs. Temperature

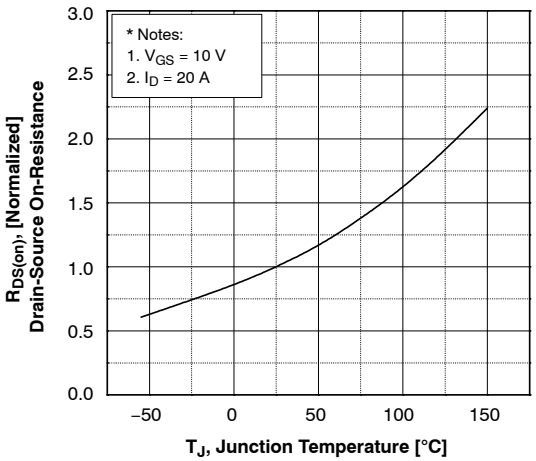


Figure 8. On-Resistance Variant vs. Temperature

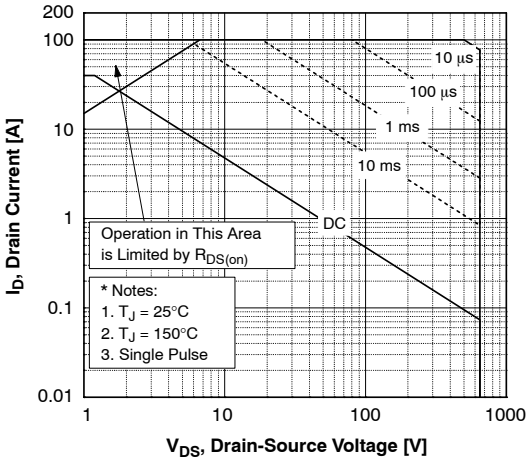


Figure 9. Maximum Safe Operation Area

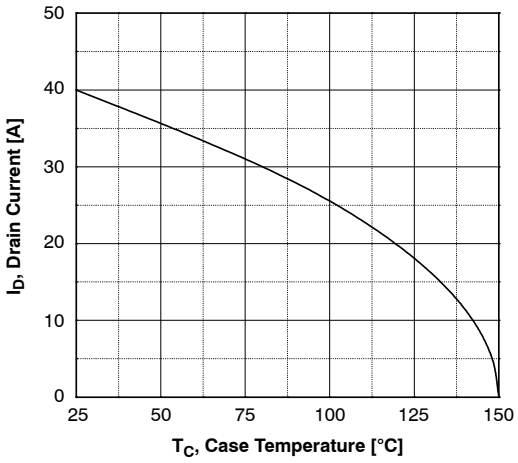


Figure 10. Maximum Drain Current vs. Case Temperature

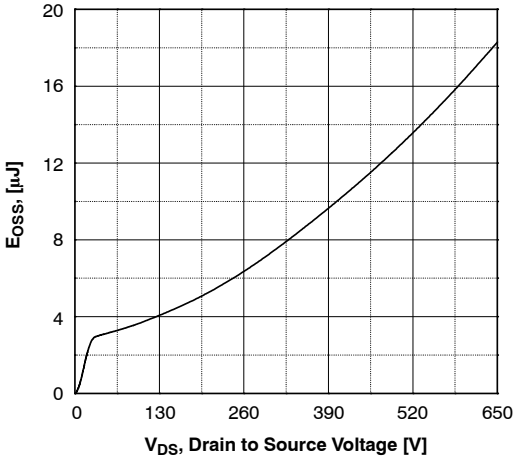


Figure 11. E_{OSS} vs. Drain to Source Voltage

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

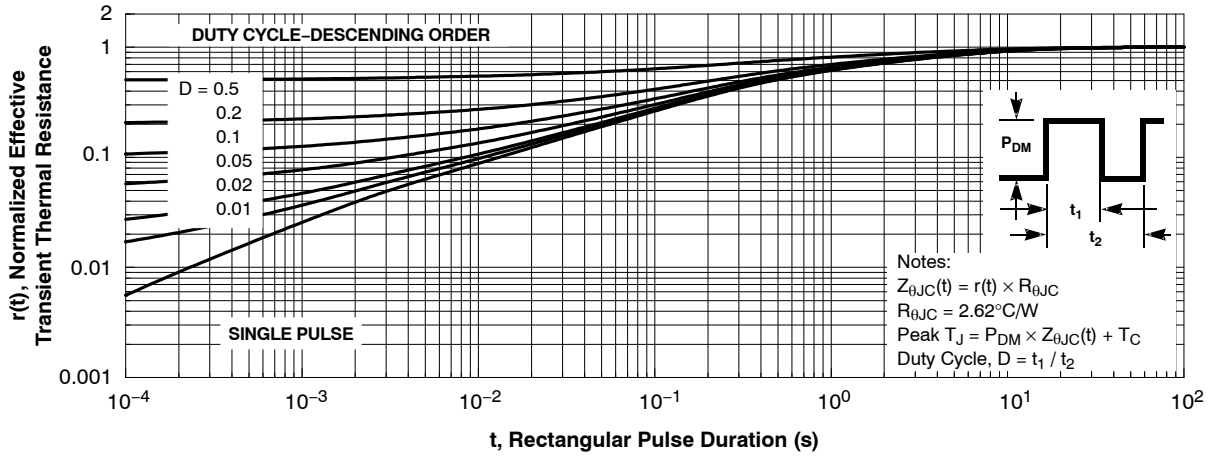


Figure 12. Transient Thermal Response Curve

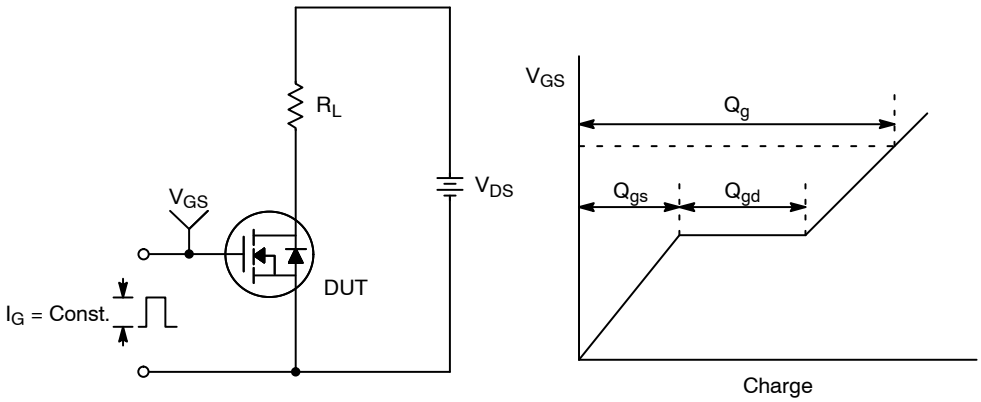


Figure 13. Gate Charge Test Circuit & Waveform

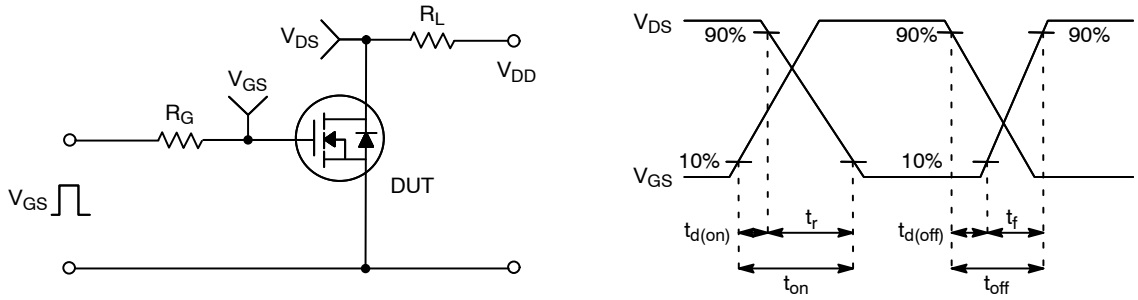


Figure 14. Resistive Switching Test Circuit & Waveforms

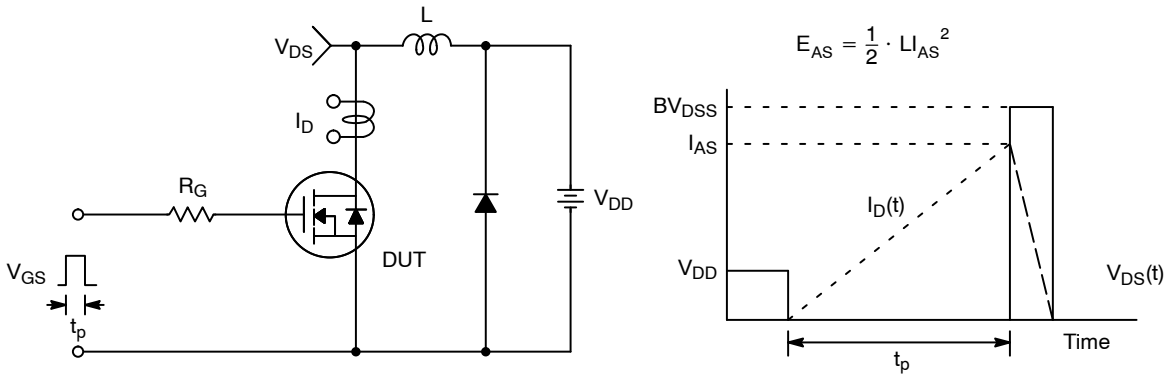


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

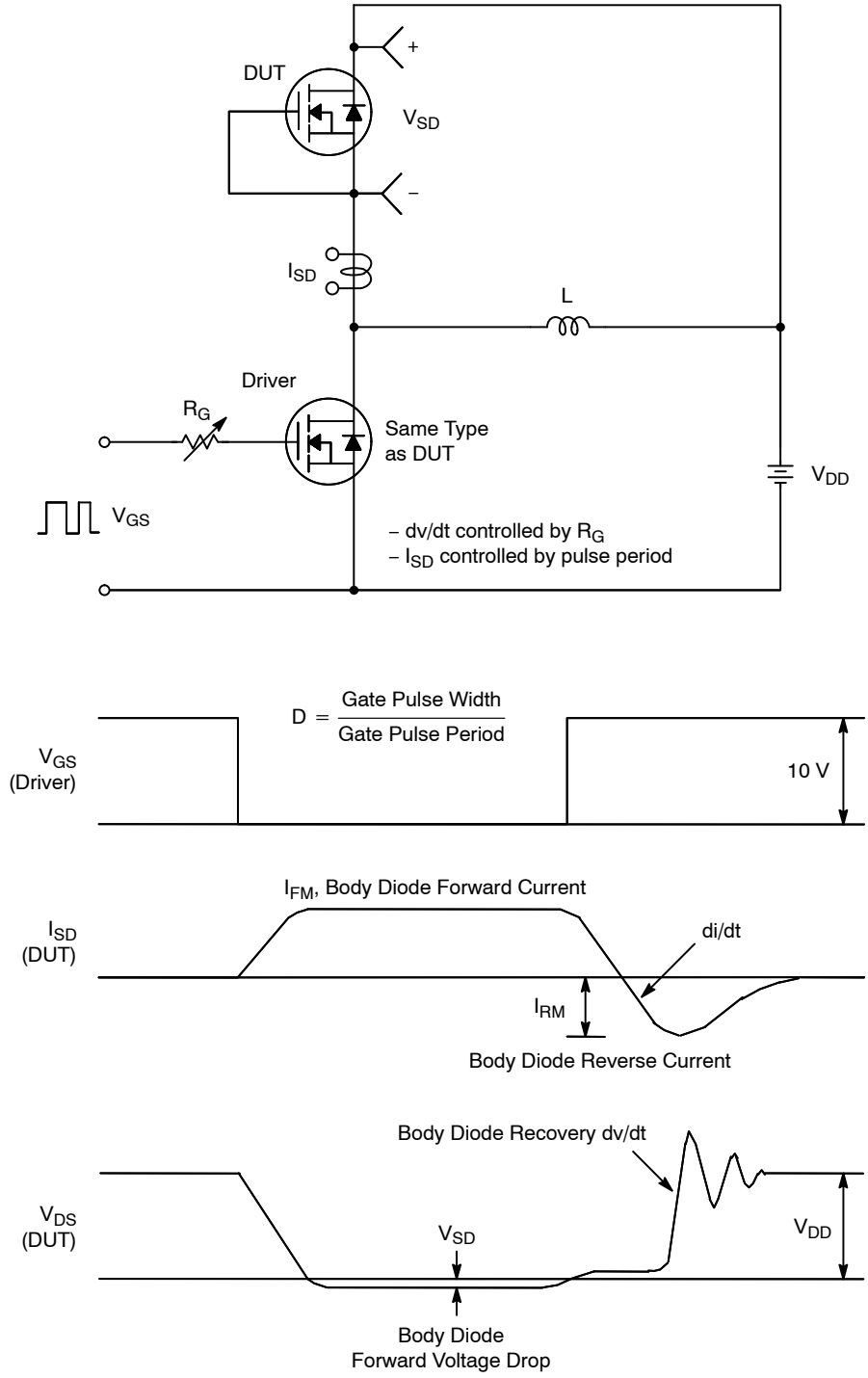
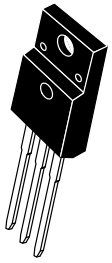


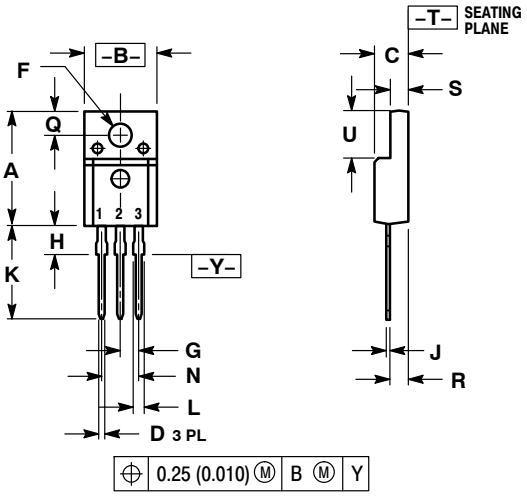
Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms



SCALE 1:1

TO−220 FULLPAK
CASE 221D−03
ISSUE K

DATE 27 FEB 2009



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH
3. 221D−01 THRU 221D−02 OBSOLETE, NEW STANDARD 221D−03.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.617	0.635	15.67	16.12
B	0.392	0.419	9.96	10.63
C	0.177	0.193	4.50	4.90
D	0.024	0.039	0.60	1.00
F	0.116	0.129	2.95	3.28
G	0.100 BSC		2.54 BSC	
H	0.118	0.135	3.00	3.43
J	0.018	0.025	0.45	0.63
K	0.503	0.541	12.78	13.73
L	0.048	0.058	1.23	1.47
N	0.200 BSC		5.08 BSC	
Q	0.122	0.138	3.10	3.50
R	0.099	0.117	2.51	2.96
S	0.092	0.113	2.34	2.87
U	0.239	0.271	6.06	6.88

STYLE 1:
PIN 1. GATE
2. DRAIN
3. SOURCE

STYLE 2:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

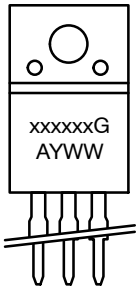
STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. CATHODE

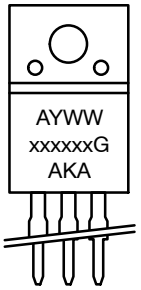
STYLE 5:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 6:
PIN 1. MT 1
2. MT 2
3. GATE

MARKING DIAGRAMS



Bipolar



Rectifier

xxxxxx	= Specific Device Code
G	= Pb−Free Package
A	= Assembly Location
Y	= Year
WW	= Work Week

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Y	= Year
WW	= Work Week
xxxxxx	= Device Code
G	= Pb−Free Package
AKA	= Polarity Designator

ISSUE	REVISION	DATE
H	REMOVED KNOCKOUT PINS FROM DIAGRAM. REQ. BY S. MASLOWSKI.	19 JUN 2006
J	CHANGED MIN AND MAX VALUES FOR SEVERAL DIMENSIONS. ADDED RECTIFIER MARKING DIAGRAM ABD PREVIOUS MARKING DIAGRAM BIPOLAR. REQ. BY S. MASLOWSKI.	07 JUN 2007
K	RE−INTRODUCED KNOCKOUT PINS INTO DIAGRAM. REQ. BY L. TSAI.	27 FEB 2009

PUBLICATION ORDERING INFORMATION

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